INTEGRATION OF SILICON NANOWIRES IN MOS TECHNOLOGY

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A THESIS SUBMITTED FOR THE DEGREE OF MASTER OF ENGINEERING
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
SILICON NANO DEVICE LABORATORY
NATIONAL UNIVERSITY OF SINGAPORE
2004

Acknowledgement:

Cette année passée à la National University of Singapore aura particulièrement enrichi mon cursus: elle m'aura permis, en effet, sur le plan technique, d'approfondir mes connaissances par la spécialisation suivie en microélectronique et, sur le plan personnel, de découvrir la culture asiatique.

En juillet dernier, j'ai été cordialement accueilli au laboratoire Silicone Nano Device Laboratory dans le département électronique et computing Engineering de la National University of Singapore afin d'effectuer, dans le cadre du programme d'échanges entre l'ENST-Bretagne et la National University of Singapore, le Double Degree Program exchange between French Grande Ecole et the Naional Univeristy of Singapore.

Je tiens tout d'abord à remercier mon maître de stage, D.Lee Sungjoo, qui m'a donné l'opportunité d'aborder le passionnant sujet que sont les nanowires-FET et qui a su, tout au long de l'année, me guider dans mon travail et me prodiguer ses conseils.

Je remercie aussi de leur concours les membres du département SNLL et les étudiants que j'ai côtoyés cette année que ce soit au laboratoire, dans les amphithéâtres, ou, pour certains, durant les séjours passés dans les pays limitrophes.

Je remercie enfin les professeurs qui ont permis d'élargir mes savoirs en microélectronique.

Cette année a été pour moi une réelle chance et je remercie l'ENST et la NUS de m'avoir fait accéder à ce programme d'échanges.

Un merci particulier à Laura qui m'a apporté son affection ces derniers mois et a eu la gentillesse de corriger la rédaction de mon travail.

This year has been very interesting for my telecommunication engineering background with a specialization in microelectronic and for discovering a new culture at Singapore. I have been welcomed in the Silicon Nano Device Laboratory in the electrical and computer engineering department of the National University of Singapore. I was doing the double degree exchange program between French Grandes Ecoles and the National University of Singapore.

First, I would like to thank my supervisor, D.Lee Sungjoo, who advised me during this year and who gave me the opportunity to deal with an interesting topic: Nanowires-FET. Eventually, I thank all teachers who taught me microelectronic during this year.

So, I would like to thank the Silicon Nano Device Laboratory department, all the teachers, staff and all the students with who I was in the lab, in Lecture Theater and for some in trip.

This year has been for me a great opportunity and I thank the ENST-Bretagne and the National University of Singapore to let me be involved in this exchange.

Julien Poizat

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Summary:

Since few years, nanowires are attractive for microelectronics to overcome the limitations of the current technology based on the silicon bulk materials. Nanowires have already been assembled in transistor which revealed pretty interesting electrical properties almost equal to the state-of-the-art of MOS process without optimization. The process to build a Nanowires-transistor was studied. Several points were highlighted: the process of the growth, the mechanism of Nanowire-FET and the issues we will have to overcome. Since the scale of the device is going near the atomic structure, some theoretical issues have been studied to know if the electrical characteristics of silicon nanowires follow the scale law. These studies have highlighted that these structures did not obey the classical law of physics.

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Abbreviations and constant

Fundamental constants :

Elementary electron charge	e = 1, 602189.10-19 C
Boltzmann constant	k_B = 1.38066.10-23 J/K
Planck constant	h = 6.62618.10-34 Js
Electron weight	m^-_e = 9.10953.10-31 kg
Velocity	c = 2.997925.10$_8$ m/s
Dielectric permitivity	$\varepsilon_{s\,0}$ = 8.854.10-12 F/m
Magnetic permeability	μ_0 = 4_.10-7 H/m
Elementary charge	q=1.60218 . 10-19 C

Abbreviations :

A*	Richardson constant
Cox	equivalent capacity at the gate oxide
D	diffusion coefficient
Dox	thickness of the buried oxide
Ec	value of the conduction band
Ev	value of the valence band
Ef	Fermi level
e_{ox}	thickness of oxide layer
G_∞	energy of volume per atom of the bulk material in a given phase
G	energy of volume per atom of the particle in a given phase
Hm	molar enthalpy of fusion
j_{ds}	density of the current in the nanowire
L	gate length of the gate
Ld	Debye length
m*	Effective mass
Nc	the equivalent density of states in the conduction band
N_d	concentration
Re	Reynolds number
Vsat	saturation velocity
σ	conductivity
l	mean free path
γ	surface tension of the liquid
θ	contact angle between the liquid and the template
σ_{LV}	liquid-vapor interface free energy,
V_L	molar volume of the liquid,
σ	vapor phase supersaturation,
R	gas constant
T	temperature.

ρ	gas density
ρ_{Si}	resistivity of Silicon
η	gas viscosity
u	gas velocity
μ_i	Fermi energy
μ_p	hole mobility
μ_n	electron mobility
Φs	surface potential
ε_r	relative permittivity of Silicon
$\Psi s1$	tsurface potential of back gate
$\Psi s2$	surface potential of wire

I. Introduction:

In 50 years, from ENIAC to microprocessor, an elementary operation is done one million times faster, requires 100000 times less power, with a price and a weight of machine divided by 10000. Compared to the other areas, the progress of microelectronics is tremendous. Moreover, whereas the other area aims seem to be limited to mere improvement of the current technology, the edge of microelectronics improvement seems to be limited only by our imagination.

Today, based on the silicon and with the state-of-the-art MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) combined with the CMOS (Complementary Metal-Oxide-Semiconductor) technology, microelectronic has become an indispensable actor in the worldwide economy. During 20 years, efforts have been done to improve the performance and the integration of this elemental device such as MOS-FET.

Still, after two decades of miniaturization, industry has to overcome other hurdles that are not only due to their realization but also some theoretical issues raised and the quantum phenomena became important.

As the integration of electronics on semiconductor, which allowed to replace the vacuum tube, we may see a mutation of current devices. Thus, it may require a technological breakthrough to go on the improvement. Especially, using a different approach to build MOS device and using the quantum effects may be a solution for the future of nano-electronics.

Among the new devices that have come up over the past year, the use of nanowires as channel appears to be a promising approach. These devices may take advantage of the confinement of the electrons to get improved electrical characteristic. At

the age of all in silicon, this device may be all the more interesting since they will be compatible with the current process in industry. Thus, building nanowire-FET based on silicon may open door to hybrid technological devices combining the CMOS technology and the advantage of the confinement of electrons in nanowires.

Many nanowires-FETs have already been built and have already proved their potential. This study is composed of:

- The first part will highlight the motivation of this work. Thus, we will present the different hurdles that the current CMOS technology has to overcome.
- Then, we will survey the different nanowires-FET already built and explain their working principle.
- We will describe the process required to build a nanowire-FET and explain the growth of nanowires.
- Then, we will describe the issues we will have to overcome during the process and will perform a theoretical study of the effect of interface states on nanowires.

II. Death of CMOS Technology:

II.1. Miniaturization:

Progress of micro-electronics, which started half a century ago, has shown the benefit of miniaturization: more transistors, higher frequencies, more reliable and cheaper. The Moore Law described the miniaturization phenomenon in 1965: number of transistors per centimeter square doubled every two years [1]. This law has become the rule of micro-electronics industry. As a result, the companies now produce circuits at nanometer size. The semi-conductor Industry Association draws lines that big companies have to follow to improve their production rate. The International Technology Roadmap for Semiconductors [2] is a sum-up of this work. Thus, Gate length is expected to be 10 nm by 2016 (fig II-1).

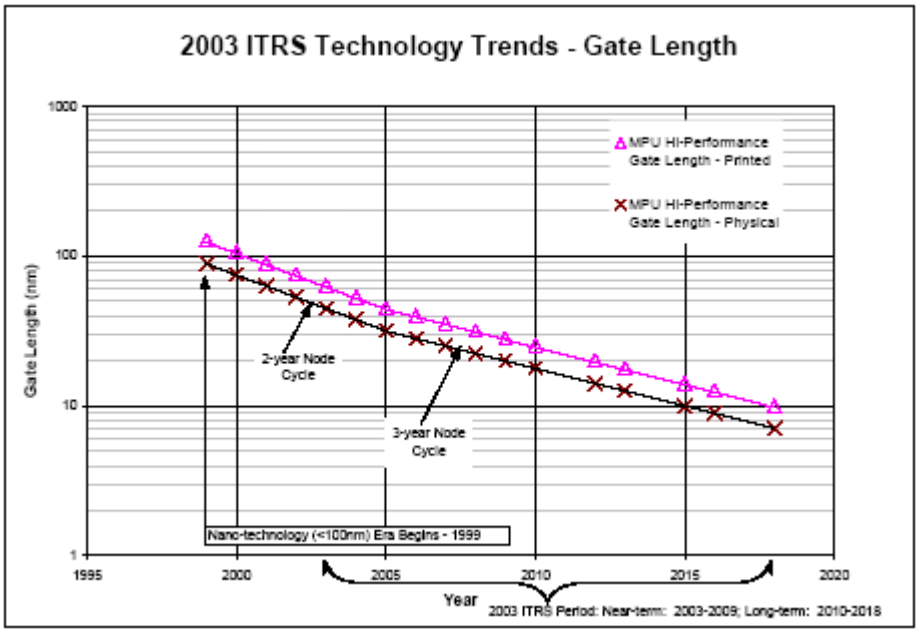


Figure II-1: 2003 ITRS-Gate length [2]

Looking at the form of equation of MOS device performance, the gate length appears to be an important parameter to increase the performance of devices. By decreasing the gate length, the drive current will be increased. However, in the next section, we are going to see that this reduction will unveil some technological as well as theoretical issues.

II.2. New issues:

II.2.1. Short channel effect:

Up to now, semiconductor industry efforts are focused to decrease the transistor gate length in order to improve the electrical performance of devices, and to increase the integration density. This is what we can observe from the evolution of DRAM (dynamic random access memory). However, this gate length decrease is performed by decreasing the others parameters of the devices. Indeed, if the gate length decrease will allow us to improve the drive current in the on state (Ion), it must not increase the off current or decrease the drain conductance in saturation regime. These effects due to the decrease of the gate length or others parameters are called Short Channel Effects and cause a reduced control of channel conductivity by the gate voltage.

Indeed, by decreasing the gate length, the drain and source region come closer and make the associated space charge regions closer. When Drain voltage becomes higher, the space charge region of Drain spreads and can join the space charge region of Source. Consequently, the potential barrier at the edge of source and substrate decreases and allows the majority carriers from source to diffuse into the substrate (figure II.2). Diffusion current is raised as soon as these carriers flow towards the drain region through

the space charge region of drain-substrate: this is the punch-through phenomenon. This overlapping of these both space charge regions lowers the barrier potential, thus disturbing the control through the Gate voltage of fixed charge in the depletion region under the gate. This lack of control in Off-state will increase the drain conductance in saturation region and decrease absolute value of threshold voltage.

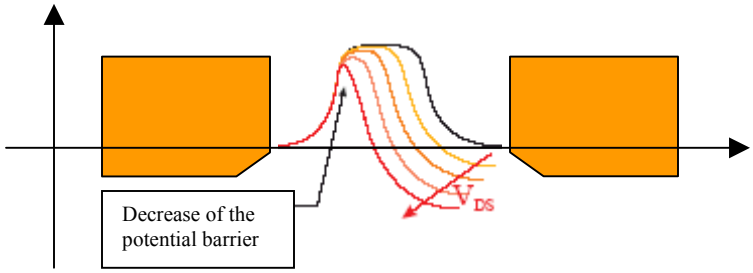


Figure II-2 : Illustration of the pinch-off phenomenon

To sum-up, this short channel effect tends to make the gate control difficult with an increase of Off-current and the conductance in saturation regime, and tends to create a dependence of threshold voltage on Vds. One solution to improve the control of the gate is to reduce the thickness of the dielectric layer to increase the equivalent capacity. Nowadays, industry tries to keep a ratio Lg/eox (oxide thickness) between 40 and 50 in MOS circuits [3]. However, the reduction of the oxide thickness will decrease the electrical-breakdown voltage of this layer.

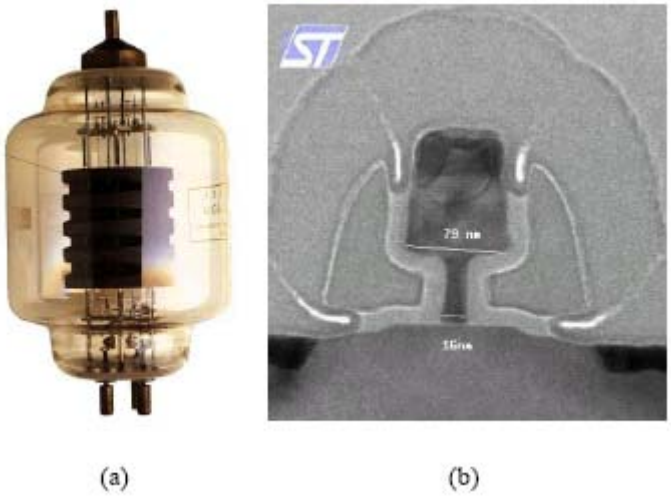


Figure II-3: Triode lamp (a), MOS transistor (b) (Lg=16 nm ST Microelectronics) [4]

The oxide thickness is not the only parameter we can modify to reduce short channel effects. To increase the substrate doping is a good way to reduce the spreading of the space charge region. However, this solution will decrease the mobility of carriers through the channel, and strongly affect the threshold voltage.

The junction depth of source/drain region can be reduced too. Still, this decrease induces a decrease of the surface perpendicular to the carrier flow; the resistance of this source/drain region tends to increase.

The terrific reduction of dimensions in MOS devices pointed out the evolution of micro-electronics. In half century, the technology has evolved from ENIAC dealing with 5000 additions per second to Pentium 4 dealing with 5000 millions of instructions per second (fig II.3). In the mean time, from the macroscopic triode, we went to MOS transistor in nanometer scale. However, this nano-scale evolution raises new issues.

In addition to the lithography issues we have to overcome before an industrial way, these nanoMOS raise quantum issues that were negligible up to now.

II.2.2. Quantum effects:

With the reduction of the gate length, the oxide thickness is decreased to improve the control of conduction channel. Thus, for MOSFET with a gate length of 30 nm, the oxide thickness is decreased to 0.8 nm [5].

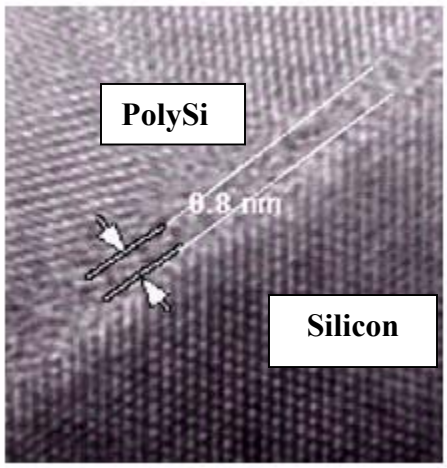


Figure II-4: cross section of MOS capacitor whose oxide thickness is 0.8 nm [5].

At this thickness, corresponding to a few atomic layers, the uniformity of the oxide thickness across the channel is difficult to achieve since it requires a control to the level of an atomic layer. The variation in the thickness of this oxide layer can lead to some weakness that reduces the maximum electric field that the oxide can endure. This lowers the integrity of oxide in high field. This effect can get worse due to the penetration of dopants coming from p+ polysilicon gate. With thickness below 2 nm, oxide becomes sufficiently low to allow the carriers to cross the oxide by tunneling effect. This phenomenon creates a gate tunneling current that is even larger since the oxide thickness is decreased. These new quantum effects modify the electrical characteristics of MOS device. Particularly, the gate tunneling effect causes an increase of Off-state current and consequently, of dissipated power. It also disturbs the On-state current since the carriers

in the channel can escape from transistor through the oxide. However, this issue is not so critical in the current device. But, as current is exponentially dependent on the oxide thickness, the gate tunneling current is one of the major drawback in the next years. Among the solution, using high-k dielectric may overcome this issue; these new dielectrics allow us to keep a good control of the channel for layer thicker than those used with Silicon oxide. Still, these new dielectrics have to face the same issue the industries have met during 35 years: difficulty to get a good insulator/Si interface [6].

Another problem that designers of nano-MOS have to overcome is the different doping required to counter the short channel effect. On one hand, the realization of complex doping profile in smaller and smaller devices is technologically difficult, especially if we want to avoid characteristics dispersion from wafer to wafer. On the other hand, the meaning of doping for such small dimension is under discussion. Indeed, for a substrate doped at 10^{18} atoms/cm^3, a channel 20*20*20 nm^3 will have only 8 impurity atoms. In that case, continuous and homogeneous doping seems to be difficult to realize. So, the discrete characteristic of impurities should be taken into account [7].

II.3. Energy issue:

One of the recurrent problems in CMOS devices nowadays is the dissipated power. This power can be divided into three different parts:

- One from Off current; short channel effect and quantum phenomena make it worse.
- One from the short-circuit current. In theory, CMOS technology avoids the simultaneous conduction of N & P type to prevent from being short-

circuited. However, with the increasing frequency of signal, time during which the P & N devices are in conduction simultaneously is not any more negligible compared with the commutation time.

- Eventually, the most part of the dissipated power comes from the energy required to charge and discharge the equivalent capacity.

Now, we will try to determine a simple equation for this dissipated power related to the characteristics of MOS devices [8]. The power dissipated through a MOS in charge/discharge capacitors C:

$$P_{dyn} = CV_{dd}^2 f \quad \textbf{(II-1)}$$

So, for Np doors, the dissipated power is:

$$P_{dyn} = N_p CV_{dd}^2 f \quad \textbf{(II-2)}$$

As we can notice through the above equation, to reach higher frequency will increase as well the dissipated power. So, in the MOS technology, to decrease the power, the V_{dd} should be decreased. However, this voltage cannot be decreased too much in order to differentiate the different signals compared to noise in circuit. This issue may become, in the future, a major problem and may be even more difficult to overcome than those related to miniaturization.

Now, to know if the current technology can be efficient to decrease this consumption, take into account a NAND and try to determine the minimum energy required to work this gate. The NAND can be seen as two bits in entry to come up with an out-bit. This process can be expressed thermodynamically by the first thermo dynamical identity [9]:

$$\Delta U = \Delta F + T\Delta S \quad \textbf{(II-3)}$$

Where ΔF represents the energy variation, that is to say the part of the total energy that can be kept reversibly, and ΔS is the entropy variation related to the energy $T\Delta S$ lost by the system. In an ideal system, the consumption of NAND will be: $T\Delta S$.

As there are two final states for four initial states, the global loss of entropy:

$$\Delta S = k_b \ln(2) - k_b \ln(4) = -k_b \ln(2) \quad \textbf{(II-4)}$$

Consequently, the minimum energy required is $k_b T \ln(2)$ within one cycle to compensate the loss of information (k_b is the Boltzman constant).

Thus if we take a Pentium 4, which consumes at rough estimate 100W in one million logic cells at $1\,Ghz$, we can evaluate the one cell consumption is about $10^8\ kT$. How to reduce this energy?

To better understand this, the power equation can be deduced. To get it, the equation is based on the following expression $P = R_c I^2$ where I is the current flowing between source and drain and $R_c = L_g / (\sigma S)$ is the channel resistance with length Lg, surface S and conductivity σ. The conductivity can be expressed as $\sigma = en\mu_n$. The mobility μ_n quantifies the ease of electron to move in presence of electric field. If we divide the velocity of electron into a drift $\vec{v}_d$ part related to the global movement due to electric field and into a part $\vec{v}_{col}$ related to the movement of electron under the thermal energy or collisions, we can write that $\vec{v}_d = -\mu_n \vec{E}$ whereas kinetic energy $m\vec{v}_{col}^2 / 2$ can be evaluated with the thermal energy $3kT/2$. Moreover, mobility is related to average time $\tau_{col} = l_{col} / v_{col}$ (l_{col} is the mean free path) between two successive collisions through $\mu_n = e\tau_{col} / m$. Thus we can deduce the expression Rc:

$$R_c = \frac{L_g}{\sigma S} = \frac{L_g^2}{Ne\mu n} = \frac{L_g^2 m}{Ne^2 \tau_{col}} = \frac{L_g^2 \tau_{col} 3k_b T}{e^2 N l_{col}^2} \quad \textbf{(II-5)}$$

The current I in the transistor is obtained from the current density $\vec{j} = -en\vec{v}_d$ in the channel so that by replacing n by $N/(SL_g)$ and by introducing the required time Δt for an electron to cross the channel with a length L_g, we got:

$$I = \|-nevS\| = \frac{Ne}{L_g} v_d = \frac{Ne}{\Delta t} \quad \textbf{(II-6)}$$

So, we can write the following expression of the dissipated power:

$$P = R_c I = N\left(\frac{L_g}{l_{col}}\right)^2 \left(\frac{\tau_{col}}{\Delta t}\right)^2 P_{col} \quad \textbf{(II-7)}$$

where $P_{col} = 3kT / \tau_{col}$.

Through the above equation, we can deduce different way to decrease the consumption of devices used nowadays in industry:

- To increase Δt may be a first solution, which comes to decrease the frequency.
- Another way is to decrease the gate length so that it becomes smaller than the mean free path or in the same way, to improve the mobility of carriers and thus increase the mean free path.
- Eventually, another way is to reduce the number of carriers N.

So, all these issues, either technological or theoretical, drive industry to create new devices to modify one of the above parameters. Moreover, industry tries to take benefits of these quantum phenomena, parasitic up to now, which appears in nanometer

devices to develop new devices. In the next part, we will describe briefly some new devices.

II.4. New devices

II.4.1. HEMT

First concept comes from forbidden gap engineering. It is to associate with different semiconductor forbidden bandgaps to create discontinuities in conduction/valence band. Especially, HEMT SiGe/Si/SiGe offers good performances at high frequencies, due to transport related to HEMT (High Electron Mobility Transistor) structures and due to the high mobility of electron in constrained Silicon between two layers of SiGe. Even if this kind of structure is good solution to improve transport characteristics, it doesn't solve the drawbacks due to short channel effect.

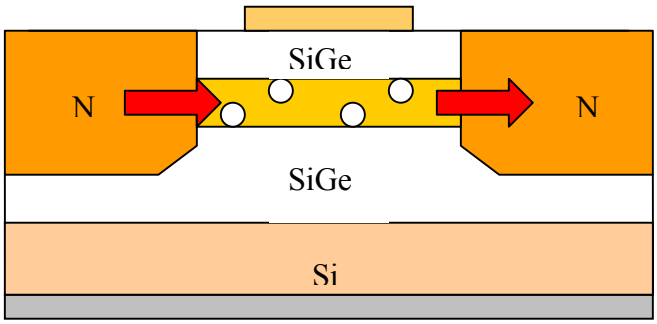


Figure II-5: HEMT SiGe/Si/SiGe

II.4.2. SOI:

Another solution is the SOI technology (Silicon On Insulator). It is compatible to CMOS technology. It consists of building a transistor over a thin Silicon layer

(nanometer), separated from the substrate by a Buried Oxide. The main advantage is the decrease of the substrate current. In such device, the drain voltage can induce short channel effect through buried oxide.

II.4.3. Multi-gates:

This technology raised new structures, in which channel is driven by several gates. If the thickness of silicon between gates is small enough, the gate voltage can control the gate in volume. Thus, the conduction is no longer at the surface but in volume, so Ion should be affected positively. These multi-gates devices are under active research, and the size of active area can reach some nanometers. So the main drawback is their fabrication that requires much superior lithography performance.

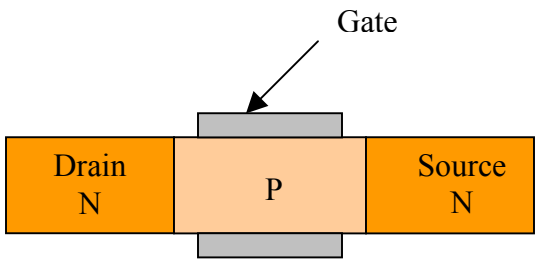


Figure II-6: Double gate scheme.

II.4.4. Molecular electronics:

The molecular electronics is a completely different approach from classical MOS devices. The approach consists of introducing molecules between two gates. The first work in this domain happened 30 years ago, the main hurdle is to synthesize them, to make interconnections and the reliability of such device. Even if this technology is far from its maturity, it has already proven several functionalities such as interrupter, diode, and memory.

II.5. Summary of this chapter

All these new devices appear really interesting to enter in the world of quantum regime, still all of them have important drawbacks. These drawbacks are short channel effects, issues due to fabrication especially due to the lithography requirement, and their unexpected behaviors.

The question now is: which devices will allow us to enter in this quantum regime with fewer drawbacks to overcome. Such an approach is the topic of this report. Silicon nanowires seem to be a good approach to overcome theses drawbacks and study the quantum effect in near term, and can be considered as a potential device for industry. Indeed, Silicon nanowires-FET consists in replacing the bulk channel between Source and Drain by introducing silicon nanowires. This device shows enhanced mobility that may decrease the power consumption. Moreover, their quantum size is obtained without any lithography method and the quality of Silicon structure is excellent. Moreover, due to their structure, the confinement of electron is higher than the others devices and can unveil tremendous characteristics due to the two dimensions confinement. So, in this report, we will explain the benefits of this new structure.

This chapter gives details on literature research on new devices and the issue raised by the quantum effect.

III. Review of nanowires:

The idea of nanowires was born in 1965 when Wagner and Ellis managed to grow Silicon whiskers with a chemical process, Vapor-Liquid-Solid method. Recently, due to breakthrough in nanotechnology, some groups were able to grow silicon whiskers at nano-scale, so-called nanowires. In this part, we will make a brief overview of the history of this method. Then, a literature review will be performed to be aware of the perspective that these new materials may offer in the future.

Nanowires are attractive for nano-sciences studies as well as for nano-electronics. Nanowires compared to other materials have electrons confined in two quantum directions, leaving one unconfined direction for electrical conduction. At this dimension, nanowires are expected to unveil different electrical properties from their bulk material. The high densities of state, diameter-dependent bandgap are just some clues that how nanowires differ from their bulk materials. Nanowires have the advantage that some properties may be controlled such as the bandgap. Driven by the smaller and smaller length scales being used in semiconductor, the nanowire research area has developed dramatically in the last years. So, we will make a brief review of the different ways to synthesize nanowires.

In this part, is presented a survey of the synthetic approaches that lead to high quality nanowires. We will review the template assisted synthesis method and the VLS method.

III.1. Template assisted synthesis:

The template-assisted synthesis consists of very small cylindrical pores or voids in host materials and the empty pores will be filled with the desired materials to form nanowires [10]. Thus, the morphology, diameter, uniformity, the chemical stability have to be taken into account. The used templates materials are anodic alumina (Al_2O_3), nano-channel glass, mica films.

To form this template, an anodization may result in an oxide film that possesses a regular hexagonal array of parallel and cylindrical channels. This self-organization relies on two processes: pore formation with uniform diameters and pore ordering. The pores form with uniform diameters because of a balance between electric field diffusion that determines the growth rate of the alumina, and the dissolution of the alumina into acidic electrolyte [11]. The pores are believed to self-order because of the mechanical stress at the aluminum-alumina interface due to expansion during anodization. This method produces a repulsive force between the pores, causing them to arrange in a hexagonal lattice [12]. Some results lead to a range from 10 nm up to 200nm with a pore density in the range of $10^9 - 10^{11}$ pores/cm²[13].

There are others porous materials that can be used such as nano-channel glass which contains a regular hexagonal array of capillaries similar to the pore structure in anodic alumina with a density about 3.10^{12} pores/cm² [11], mesoporous molecular sieves have hexagonally-packed pores with very small channel diameter which can be varied between 2 nm and 10 nm [14]. Recently, the DNA molecule has been used for growing nanowires [15].

III.1.1. Pressure injection method

To form nanowires, the pressure injection technique is used with a low-melting point material or when using templates with robust mechanical strength. The nanowires are formed by pressure injecting the desired materials. Anodic aluminum oxide films and nano-channel glass used this method. Metal nanowires (Bi, In, Sn an Al) and semiconductors nanowires (Se, Te, GaSb and Bi2Te3) have been fabricated with this method [16].

The pressure required to overcome the surface tension for the liquid material to fill the pores with a diameter is determined by the following equation:

$$d = -4\gamma\cos\theta/P \quad \textbf{(III-1)}$$

Where γ is the surface tension of the liquid, and θ is the contact angle between the liquid and the template. To reduce the required pressure and to maximize the filling factor, some surfactants are used to decrease the surface tension and the contact angle.

III.1.2. Vapor deposition method

Another way to deposit the materials into the pores is the vapor deposition method which includes Physical Vapor Deposition [17], Chemical Vapor Deposition [18]. This method allows us to get smaller diameter than the pressure injection method since it does not rely on the high pressure required in the former method. In this method, the material is heated to produce a vapor that is introduced through the pores of the templates and cooled to solidify. Single-crystal Bi nanowires in anodic aluminum templates with pore diameter as small as 7 nm have been fabricated [17].

The method that I will introduce now is the one expected for our project: VLS method. This method has already been introduced in 1965 by Wagner and Ellis, this mechanism allowed them to get the growth of single crystal silicon whisker 100 nm to hundreds of microns in diameter. Recently, Harvard group has successfully grown Germanium and Silicon nanowire [19] and, has managed to grow a multi-shell nanowire based on this method. In this project, we want to focus in this method with the use of Chemical Vapor Deposition.

III.2. Vapor liquid solid method:

This growth mechanism is based on the consumption of source materials from the gas phase into a liquid droplet of catalyst. Berkeley group has successfully observed the VLS nanowire growth [20], [27], [28]. Based on these observations, we can identify three process steps:

- Alloying Process: Ge and Au clusters, which act as catalyst, form a liquid alloy as soon as the temperature reaches the eutectic point. Indeed, with the increase of Ge vapor, the alloy composition crosses a biphasic region (solid Au and Au/Ge liquid alloy) and a single-phase region (liquid)
- Nucleation: By increasing the amount of Ge (weight), it reaches another biphasic region. (Au/Ge alloy and Ge crystal), the nucleation starts. As for Ge, they estimated that the nucleation generally occurs at Ge weight percentage of 50-60%.
- Axial growth: Further amount of Ge vapor into the system will increase the precipitation. The incoming Ge species rather diffuses and condense at the solid/liquid interface based on the lever rules of phase diagram (figure III.1).

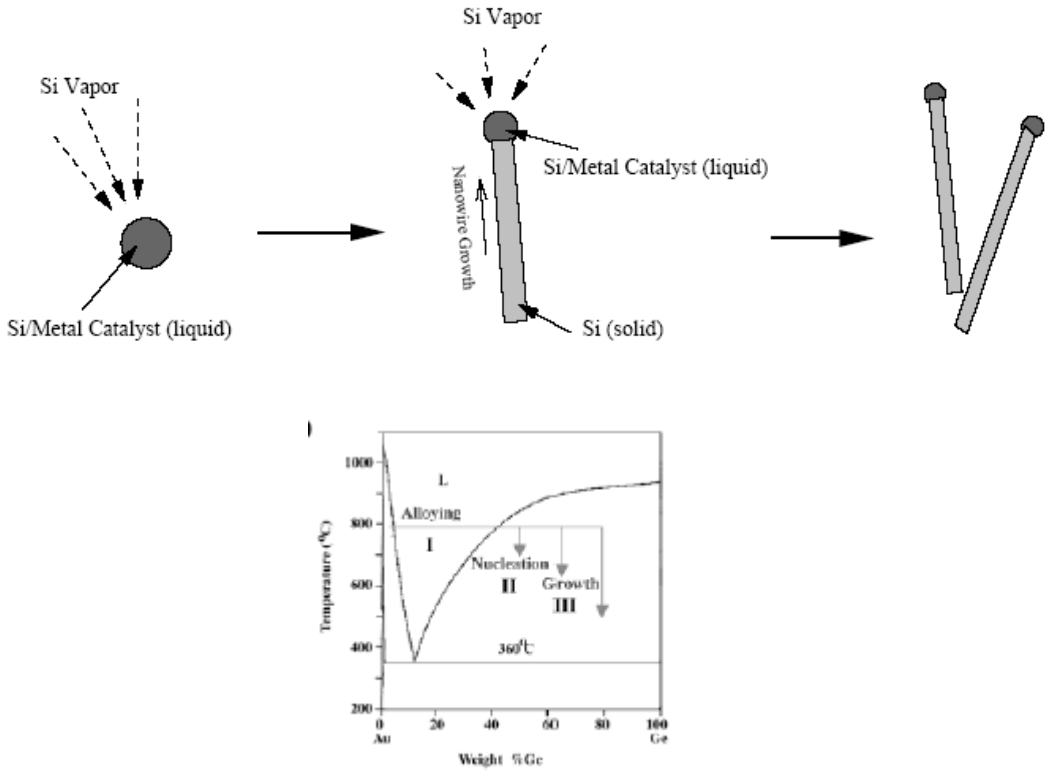


Figure III-1: Illustration of Vapor-Liquid-Solid nanowire growth mechanism including three stages alloying, nucleation and axial growth [20].

The nanowires fabricated through this method are of high purity except for the end containing the catalyst. A wide variety of compound semiconductor nanowires has already been synthesized via this method [24], [25], [26], [31]. Many groups, especially by Harvard group, have performed a good control over the diameter and the distribution. Recently, some groups have managed to grow nanowires with different materials and they control the materials along the nanowires to get a compositionally modulated nanowire. Thus, p-Si/n-Si nanowires were grown by chemical vapor deposition from alternating gaseous source containing the appropriate the dopant.

III.2.1. Catalyst:

Experimentally, a linear correlation can be extracted:

$$D_{wires} = D_{clusters} + 5\,\text{nm}$$

So to achieve reduction of the average wire diameter (D_{wires}) to the nanometer scale requires through this method the generation of nanosized catalyst with small diameter ($D_{clusters}$). There are several technologies to get them:

- Monodispersed nanoparticles are commercially available (Ted Pella), they can be dispersed on a solid substrate in high dilution so that when the temperature is raised above the melting point, there is no aggregation.
- Laser assisted catalytic is used to generate nanowires under non-equilibrium conditions. So the laser ablation method can be used to generate nano-sized clusters of virtually any materials. [21]

Different catalysts used with their eutectic temperature:

- Gold is most used, Au/SI: 450C, Au/Ge: 380C, Ti-containing islands. [22], Zn [23], Ti/Si: 1300C, Fe/Si: 1207C

Catalyst acts as a favored reaction site that is localized at the end of the nanowire. As we can see through different experiments, the diameter of the nanowire is determined by size of the cluster. So, by using binary alloy phase diagram, we can choose catalyst that allows to get material nanowire desired. Then, the phase diagram is used to determine the temperature and catalyst ratio to get the coexistence of liquid alloy and solid nanowire material.

In this view, we can imagine to grow any type of nanowires. However, under thermal equilibrium, catalysts form cluster with a radius determined by the following equation:

$$r_{\min} = 2\sigma_{LV} V_L / RT \ln(\sigma) \quad \textbf{(III-2)}$$

σ_{LV} is the liquid-vapor interface free energy,

V_L is the molar volume of the liquid,

σ is the vapor phase supersaturation,

R is the gas constant and

T is the temperature.

Through the literature, groups who have followed the VLS method, only got micrometer diameter whiskers.

Methods that constrain the catalyst cluster to diameter in the 10 nm size range exist and hence enables the growth of nanowires. A straightforward approach to produce such small clusters is laser ablation and condensation, which have been studied extensively in the past to generate nanometer diameter clusters. This method is Laser-assisted Catalytic Growth (LCG).

Otherwise, some nanoparticles are commercially available with different diameter (Ted Pella, British Biocell). These particles are stabilized by different ways. To stabilize this solution, we need forces. Two different forces are mainly used: Electrostatic force and steric repulsive force. The electrostatic force is the effect on particle interaction due to the distribution of charged species in the system, thus simply altering the concentration of ions in a system may modify the stabilization of a system. In this view Zeta Potential is a very good index of the magnitude of the interaction between colloidal particles and Zeta Potential measurements are used to assess the stability of colloidal systems. The steric repulsive force involves polymers added to the system adsorbing onto the particle surface and causing repulsion. It is a simple process requiring just the addition of a suitable polymer.

III.2.2. Binary Phase diagram

With the reference book [24], we can have a view of the different catalyst materials we can use.

Two considerations must be taken:

- Temperature of the eutectic point.
- Material should be C-MOS compatible.

We can select as C-MOS compatible materials; Zn, W, Ti, Pt, Pd, Ni, Mo, Hf, Ag and Au. Through the literature, growth of nanowires has been performed with Au, Zn, Ti.

For Au, the process is well known. However Au presents some drawbacks with C-MOS process due to its diffusion in Si. As for Zn [23], UCLA has reported in 2000 the growth of Si-NWs using Zn as catalyst. Looking at the phase diagram provided, the eutectic point is located at 420C with 99 per cent of weight percent Zinc.

As for Ti, HP has performed the growth of Silicon nanowires with TiSi2 catalyst. However, as we can see through their results, the quality of nanowires is not satisfactory. Through the different C-MOS compatible materials, we should study their characteristics with Silicon from Quick reference manual for silicon integrated circuit technology / W.E. Beadle, J.C.C. Tsai, R.D. Plummer, editors New York : Wiley , c1985 [30]

C-MOS Compatible materials	Eutectic point temperature degree Celsius	Metal Silicide	Activation Energy Ev@300K	Barrier Height N-Type and P-Type EV	
Zn	419.58				
W	1392	WSi2	2.5	0.65	
Ti	1330	TiSi2		0.6	0.6
Pt	979	PtSi	1.5	0.84	0.26
Pd	870	Pd2Si	1.12	0.84	0.26
Ni	981	Ni2S	2.1	0.6	
Hf	1360	HfSi	1.6	0.4~0.5	0.9
Ag	845		0.95		0.55

Table III-1: Catalyst materials.

For reference, Au has activation energy: 0.7eV@300k. This is exactly the electromigration activation energy that has been estimated from the melting temperature of material.

Through this survey, we can note the case of Pd and Pt. Indeed, what appears really interesting is its low barrier height with p-type silicon. These are the lowest barrier height noted through this survey. Now the question is to know if we can use this material as a catalyst for growing Silicon nanowires. Referring to the phase diagram, it appeared that the catalytic favored reaction is possible with PdSi and PtSi silicide. The eutectic point is localized at 976 degree Celsius for Pt, 870 degree Celsius for Pd, and 23 weight percent Silicon for both.

The issue here is how we can form island of Silicide on the substrate.

III.2.3. CVD

The process uses Chemical Vapor Deposition. This process relies on different steps. To better understand the process, we should describe briefly the sequence of this method:

- 1 Mass transport of reactant and diluent gases (if present) in the bulk gas flow region from the reactor inlet to the deposition zone
- 2 Gas phase reactions (homogeneous) leading to film precursors and by-products (often unselective and undesirable)
- 3 Mass transport of film precursors and reactants to the growth source
- 4 Adsorption of film precursors and reactants on growth surface
- 5 Surface reactions (heterogeneous) of ad-atoms occurring selectively on the heated surface
- 6 Surface migration of film formers to the growth site

- 7 Incorporation of film constituents into the growing film: that is, nucleation (island formation)
- 8 Desorption of by-products of the surface reactions
- 9 Mass transport of by-products in the bulk gas flow region away from the deposition zone toward the reaction exit.

These are the different steps in the reaction underlying CVD process. The growth of nanowires is directly linked to the 4, 5, 6, 7 and 8 steps. The three first steps have an impact on the growth of nanowires since these steps provide the seeds for the growth process. Moreover, to understand the characteristics that may modify the nanowires growth, we have to describe the mass transport and thermal activation.

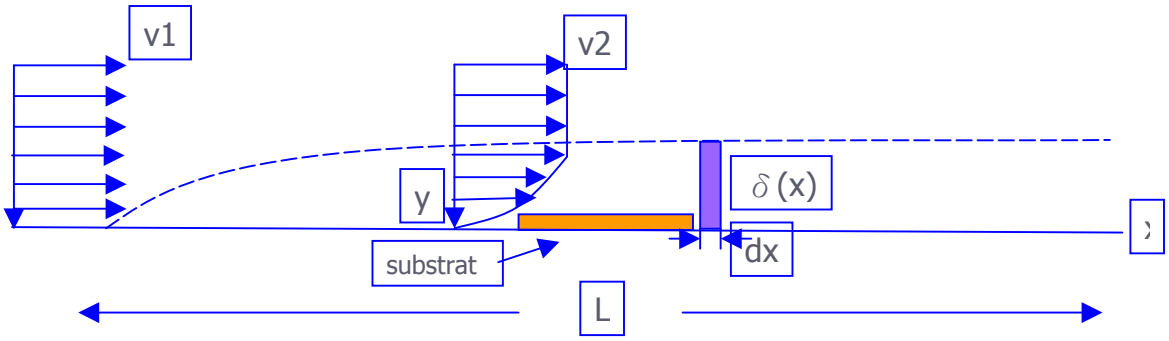


Figure III-2: illustration of the flow inside a CVD

III.2.3.1. Mass Transport:

$R_e = \rho u L / \eta$ **(III-3)**

$F = -D\delta C / \delta x$ **(III-4)**

δC/δx is the concentration gradient

$F = -D(3 * \Delta C / 2L)\sqrt{\mathrm{Re}}$ **(III-5)**

(material flux to the substrate)

ρ: gas density

η: gas viscosity

u: gas velocity

D: diffusion coefficient

Re: Reynolds number

Through this equation, to increase the seed of reactants to substrate, the characteristics we have to improve are the gas velocity that is related to diameter of the tube, the gas viscosity, the diffusion coefficient. With a material chosen, the main characteristics would be the gas velocity. So, a small diameter is required.

III.2.3.2. Thermal activation:

Surface reactions rate:

$$R = R_o e^{-\frac{E_a}{kT}}$$ **(Arrhenius law) (III-6)**

R0:frequency factor

Ea: activation energy in eV

T: temperature

To increase the surface reaction, the main characteristic to improve is to increase the temperature. Still, other considerations should be taken into account since the temperature is involved in other CMOS processes which may alter the quality of nanowires.

The main variable affecting the CVD process (refer to the figure III-3) and consequently the growth of nanowires are: Mass flow rate, temperature, pressure, reaction time.

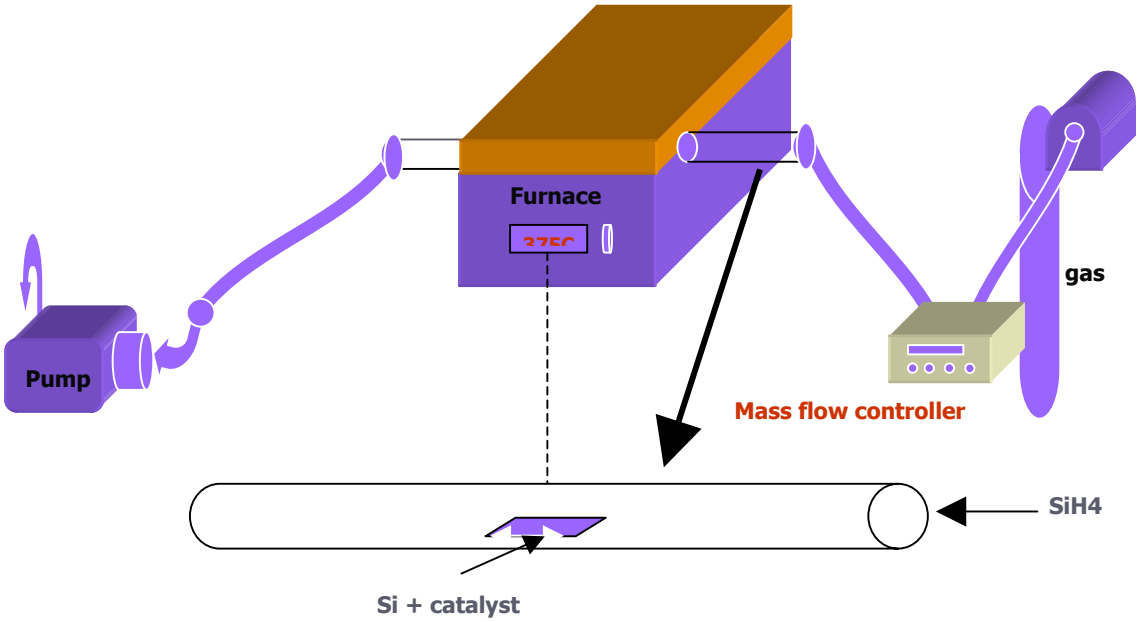


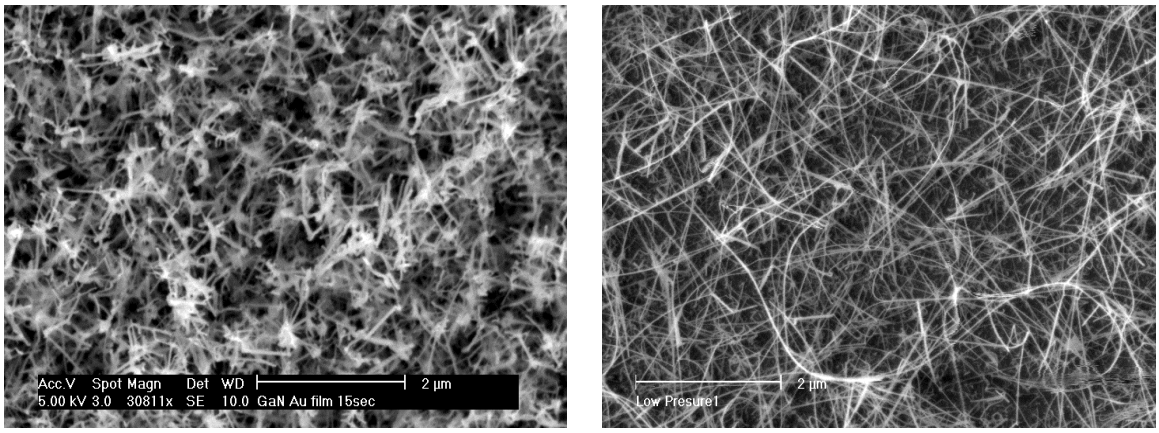
Figure III-3: illustration of a CVD machine

III.2.3.3. Impact of parameters on the growth:

In this section, we will discuss about the impact of parameters concerning the growth of nanowires. As for pressure, figure III-4 shows two different nanowire growth with different pressures. The effect of pressure is related to the concentration of materials. Consequently, increase the partial pressure of silane would increase the concentration of silane, thus a large amount will be provided to the growth valorizing not only the axial growth but also the transversal growth. Consequently, the pressure will affect not only

the length of nanowires but also the diameter, as we can see in the following pictures (figures III.4).

Further, as the amount of material will be enough, this may affect as well the uniformity of nanowire.



High pressure
10^{2}Torr

Low pressure
10^{-1}Torr

Figure III-4: nanowires at different pressures

As for the temperature, it affects the reaction rate. Consequently, as the temperature increases, the reaction rate will increase and will increase the incorporation of materials on the catalyst. Thus, the growth rate will increase. Meanwhile, as the reaction rate will increase, the transversal growth may increase as well.

We can draw the chart shown in figure III-5 to describe qualitatively the effect of pressure and temperature on the growth of nanowires.

As for the mass flow rate, as we increase, the Reynolds number will increase thanks to the equation III-3. So, the thickness of the boundaries layer will increase. Consequently, the increase of the flow will increase the diffusion of reactant through the

boundary layer. In other words, the reaction will not be limited by the diffusion of reactants through the boundaries layers. This will affect the growth rate.

The consequences previously described are only supposition and needs to be confirmed by experiments. Still, it can serve as a basis to set up our experiment.

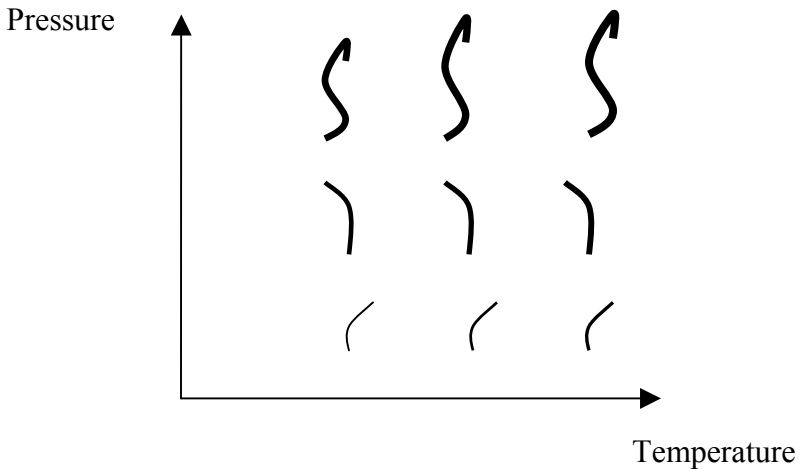


Figure III-5: Scheme of nanowires according to Pressure and Temperature

Another characteristic that may influence the growth process of nanowire is the flow of H2 used. To understand the mechanism, we have to take into account the reactions involved in. This can be called H2-assisted growth effect:

- $SiH_4(g) \rightarrow Si(s)+2H_2(g)$
- $SiOx(s)+H_2 \rightarrow Si(s)+xH_2O(g)$

Through this chemical reaction, the amount of H2 will control the silane decomposition. So, to clarify, based on the above equation, let's consider two limiting cases:

- A small amount of H2 will prevent the decomposition of Silane and will favor the formation of the oxide coating.

- On the contrary, a high flow of H2 will improve the decomposition of silane and allow the decrease of the oxide coating thickness.

These hypotheses are confirmed by the results from report [30]:

- >200 sccm: Growth of nanowire stopped
- < 50 sccm: amorphous coatings on the substrate and reactor walls
- ~100sccm to get nanowire

So, the flow rate of H2 has to be taken into account in the process as the others parameters.

III.3. Summary of this chapter:

To sum-up this part, the process involves many parameters such as the temperature, the pressure, the H2 flow rate and the mass flow rate. The growth rate, the morphology of nanowire may be modified through these parameters. Still, the growth process needs a complex process to deposit the catalyst and avoid the agglomeration of them, which would increase dramatically the diameter of nanowires. This would be discussed in the chapter IV concerning the process required to grow nanowires.

The question is now: why should we choose this way of synthesizing nanowires rather than the other previously presented. Briefly, the VLS method allows us to build nanowires virtually with any materials. The high quality of the crystal is one of the most important reason to use it, the quality is higher than the template synthesis which relies on the good quality of the templates and finally, the cost of this method is lower since it doesn't require the formation of template, neither a high pressure.

IV. Fabrication of a nanowires-FET:

To overcome the hurdle imposed by the miniaturization, the semiconductor industry has developed new devices. The recent devices that have struck our mind are the molecular one, and those based on the uses of nanotubes and nanowires.

For molecular nano-transistors, the recent breakthrough is due to the group of professor Cees Dekker (University of Delft). They managed to build a molecular transistor based on carbon nanotubes. Carbon nanotubes were developed for the first time in 1991 by Dr Sumio Iijima (NEC Fundamental Research Laboratory). These tubes are composed by a great number of benzelique cycles and look like a graphite plan which would has been rolled up; the diameter of nanotube is generally at about 1-2 nm. Several nanotubes can be incorporated in the others. This material has raised a great interest for their mechanical characteristics (The Youngs modulus is larger than that of iron) and for their electrical characteristics. Carbon nanotubes can be either semiconductor or metallic according to their diameter or the way of their rolling up. In the next part, their electrical performance will be quoted. The electrical performance is tremendous compared to the conventional MOSFET. Still, no one managed to grow only semiconductor nanotubes, since their growth gives a mix of metal and semiconductor nanotubes.

As for the molecular transistor with organic molecules between electrodes, the main issue is the weakness of material and the difficulty to synthesize interesting molecules.

Nanowires seems to be an interesting way to develop new devices since nanowires don’t experience the hurdles that prevent the two formers devices to be developed.

IV.1. Electrical results:

Since nanowires were first introduced in 1965 by Wagner and Elli, many breakthroughs have been achieved. Many groups have already built such device. So, in the following part, we will introduce a review of the different devices built based on the use of nanowires or nanotubes. Below are some characteristics of these new devices. [32], [33], [34], [35], [36]. Figure IV-1 shows the subthreshold slope of different devices, figure IV-2 points out characteristics of new devices and figure IV-3 highlights the mobility of new devices.

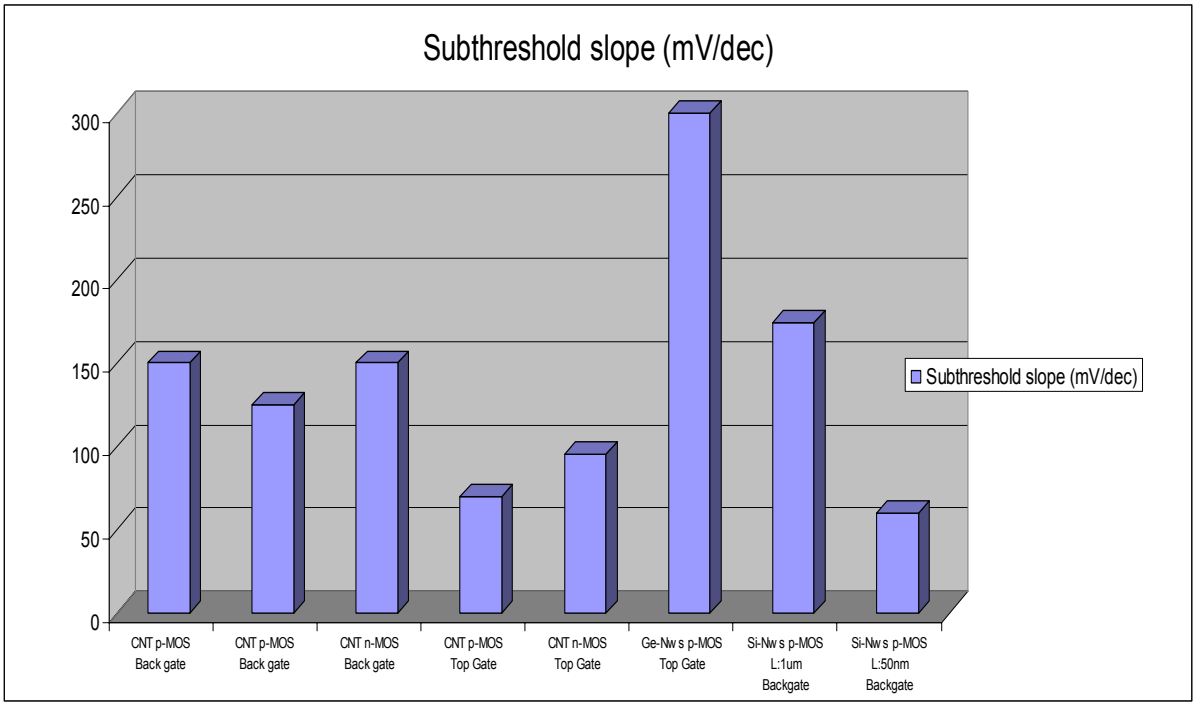


Figure IV-1: Subthreshold slope for new devices.

Group	S/D	Structure	Material	Length	Diameter (nm)	Subthreshold slope (mV/dec)	Ion/Ioff Ratio	Idsat µA per tube	Idsat normalized µA/µm	Conductance	Mobilities cm²/V·s	Transconductance S/m
Dai's group Stanford	Pd	Back gate	CNT p-MOS	275nm	1.2-5nm	150	1.00E+07	25	7000	12e2/h	4000	
Dai's group Stanford	Pd	Back gate	CNT p-MOS	3um	2-3nm	100-150	1.00E+06	20	8000	0.1-0.2*4e2/h	3400	
Dai's group Stanford	Al	Back gate	CNT n-MOS	3um	2-3nm	150	>10e4	10	3600	0.05*4e2/h	3750	
Dai's group Stanford	Mo	Top Gate	CNT p-MOS	2um	1nm	60-80					3000	6000
Dai's group Stanford	Mo	Top Gate	CNT n-MOS	2um	1nm	90-100					1000	600
Dai's group Stanford	Pd	Top Gate	Ge-Nws p-MOS	5um	20nm	300	1.00E+04	3	600		600	300
Lieber's group Harvard	Au/Ti	Backgate	Si-Nws p-MOS	1um	10nm	174	1.00E+06		50-200		230-1350	17-100
Lieber's group Harvard	Au/Ti	Backgate	Si-Nws p-MOS	50nm	10nm	60	1.00E+06		2000-5600		230-1350	2700-7500

Figure IV-2: Characteristic of new devices.

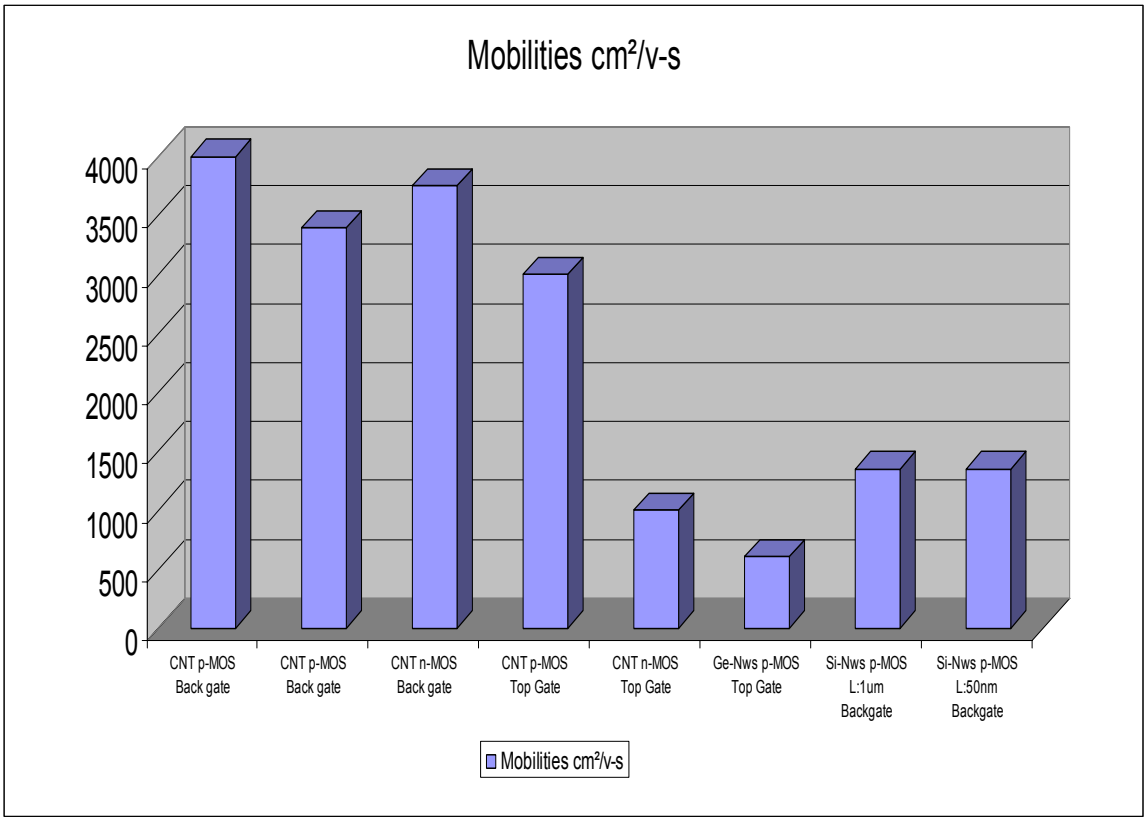


Figure IV-3: mobility of new devices.

As we can see through these charts that retrieved all the electrical data available in the recent reports, the use of nanowires appears interesting. The nanowires transistor highlighted good result at the early stage of this development. It is far from the result concerning the carbon nanotubes. Still, nanowires allow us to overcome the main hurdle of carbon nanotubes, all the nanowires are semiconductor. So, nanowires-FET is an interesting device that can suit the requirement of ITRS roadmap in the next generation, waiting for the development of carbon nanotubes or organic based devices. Indeed, the reliability of nanowires may be easier to reach.

Not only for the semiconductor industry, the development of Nanowires-FET may enhance others area. Indeed, due to the miniaturization of devices, the semiconductor

industry enters in the quantum area. At this scale, the behavior differs from the macroscopic view of the conventional MOSFET and some theories have already come up. And these nanowires may allow us to study confinement of electron in 1D material to check theoretical predictions.

The nanowires as well will allow the development:

- High speed device due to the enhanced mobility.
- Interesting TFT due to their small diameter.[37]
- New photo-electronic devices due to the variation of bandgap.

And nanowires will allow us to enter in the new device area: Single Electron Transistor due to their quantum size [38].

Now for our area, we will discuss about the benefits of this devices compared to the conventional MOSFET. Up to now, few results force us to believe that the nanowire-FET doesn't work like the conventional MOSFET. So, we will describe the way of working of a MOSFET to better understand the evidence that nano-FET doesn't work like a MOSFET. Then we will try to explain the results and infer some properties concerning the transport.

IV.2. MOSFET Behavior:

The main principle of MOSFET lies on the control of carriers flux flowing between two electrodes called source and drain with a third electrode called gate. For example, PMOS transistor is composed of doped silicon substrate (concentration N_d) on which we realized an oxide and metallic gate (e_{ox} and L representing respectively the thickness of oxide layer and the length of the gate). Then two highly doped parts P+ (N_a

concentration) that represents the source and drain. Metallic contact on these parts, gate and substrate allow to bias this device.

In such transistor, for the carriers (here holes), flow from source to drain, two conditions must be fulfilled:

On the one hand, we have to form the channel conduction between source and drain. Indeed, the two pn junctions constituting the device source-substrate-drain prevent carriers from flowing at any V_{ds} when gate is not biased. Since the channel doesn't exist at zero bias, we have to create it by applying a negative bias. The MOS capacity formed by the substrate-oxide-gate layer reacts to the amount of negative charge on the gate by repelling the electrons initially localized under the oxide towards the substrate, forming a space charge region at the interface Si/SiO_2. From a threshold voltage V_t, the space charge doesn't allow to compensate the large amount of negative charged, an inversion layer of some nanometers composed of holes coming from the source and drain appears under the oxide. The value of threshold voltage depends essentially on donors concentration, gate metal, the materials and the thickness of the dielectric.

On the other hand, once the condition $V_{gs}<V_t$ realized and a hole-channel is formed, we have to apply a bias V_{ds} so that an electric field parallel to the Si/SiO_2 interface makes holes flow in order to establish a positive current I_{ds}.

Due to this simple behavior, a PMOS can be explained by comparing it to a hydraulic scheme. This analogy coming from the reference [8] will allow us to describe easily the voltage/current characteristic of the device. For this, we can modelize the source and drain by two reservoirs of liquid whose inertia is low enough so that the flow can take

place slowly. Between these two reservoirs, there is a wall, whose height is V_t compared to the initial level of source and drain, and which plays the role of potential barrier controlling the flow. The fig IV-4 (a) represents the transistor in Off state. The first step to let carriers flow is to lower the wall to create a channel between these two reservoirs. Eventually, a differential potential should be applied so that the liquid can flow from source and drain.

In the (b) case, a low potential has been applied so that the height of drain reservoir remains higher than the wall. To calculate the current at the abscise x, we have to multiply the volume of liquid at x with its speed. If the volume at x is clearly proportional to the height V(x), its speed is proportional to the gradient –dV/dx. Indeed, more abrupt it is, the faster it is. So, the current I_d in the transistor MOS, for low value of V_{ds}, can be written with proportionality coefficient K:

$$I_D = -KV(x)\frac{dV(x)}{dx} \quad \textbf{(IV-1)}$$

with the stationary regime, the current Id cannot vary along the channel; integrating the above expression along the channel, we get:

$$I_D = \frac{K}{2Lg}\left[V^2(0) - V^2(Lg)\right] \quad \textbf{(IV-2)}$$

According to the picture, we have V(0)=Vgs-Vt and V(Lg)=Vgs-Vt-Vds, so that we get:

$$I_D = \frac{K}{Lg}\left[(Vgs - Vt)Vds - \frac{V^2 ds}{2}\right] \quad \textbf{(IV-3)}$$

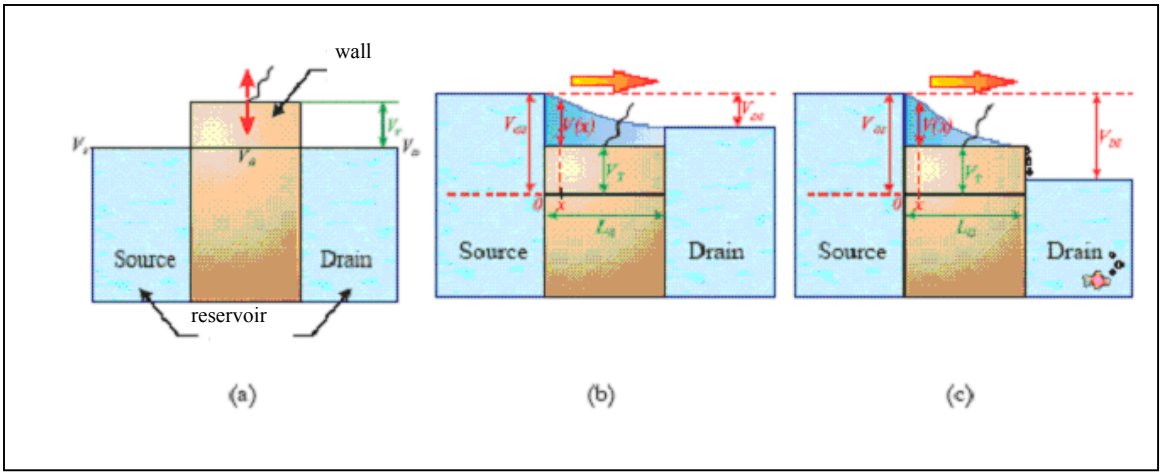


Figure IV-4: MOSFET behavior

Let us examine the case where the height of drain reservoir is below the height of the mobile wall. In such a case, the flow is not dependent on drain height: This phenomenon occurs as soon as the drain level reaches the height of mobile wall, Vds=Vdssat=Vgs-Vt. The consequence is the existence of a saturation region in which current becomes independent of Vds as Vds<Vgs-Vt<0. We get:

$$I_{sat} = \frac{K}{2Lg}(Vgs - Vt)^2 \quad \textbf{(IV-4)}$$

This simplified description doesn't allow to explain the coefficient K. This factor is given by:

$$K = \mu_p C_{ox} W \quad \textbf{(IV-5)}$$

where Cox is the equivalent capacity per unit at the gate oxide.

Besides, the equations are accurate only if the length L_g is long enough.

In the previous section, we have briefly described the operation of a conventional MOSFET. In the next part, we will try to conceptualize in an easy way the behavior of a nano-FET.

IV.3. Nanowires-FET behavior:

The nano-FET is composed of two metal gates and dielectric layer and a metal gate (refer to figIV-5 on page 42). To infer the transport mechanism of this device, we can foresee some phenomena that can be put forward in the future work. Two main behaviors can be highlighted in the future:

- Reversing Source/Drain
- Subthreshold behavior

IV.3.1. Reversing Source/Drain:

Let's consider the reversing Source/Drain behavior. An interesting experiment to do is to reverse the role of Drain and Source. Whereas it would be the same nanowire with the same voltage range, the data may differ significantly. Especially, Idsat may differ. If it was due to pinch off, this difference could not exist since the same nanowire would give the same Idsat. The main mechanism occuring at these interfaces is the tunneling through the barrier. Consequently, the probability of carriers tunneling through the barriers is strongly dependent on the voltage applied to the Source and Drain. Thus, by reversing the Drain and Source, the current may differ. As the barrier may be slightly different, carriers have more probability of tunneling through the barrier than the other side. Contrary to the conventional MOSFET where the pinch-off causes the current to saturate, it cannot explain this difference since nanowires would be the same in the experiments. In that case, we could conclude that the nanowires could not determine the electrical performance of the device by themselves.

IV.3.2. Subthreshold behavior:

Let's us consider now the subthreshold behavior. To determine if the Nanowires themselves would set a barrier to the current transport and consequently to know if the "bulk" switch phenomenon would dominate, the subthreshold should decrease for decreasing temperature. This is based on the behavior of a long channel MOSFET where the subthreshold is determined by the following equation: $S = 2.3\frac{kT}{q}\eta$ **(IV-6)**. [39]

In the case of nano-FET, we may expect a different behavior from the conventional MOSFET as previously quoted. In this case, we may encounter a saturation of the subthreshold slope at a certain temperature which indicates that the nanowires-FET is determined by the tunneling through the source Schottky barrier rather than by the thermionic current. Indeed, the current component due to tunneling does not decrease as rapidly as the thermionic component.

Moreover, we may have to take into account the effect of the gate field on the barrier of the source. Indeed, the current in the Off-state is determined by the coupling of the gate field to the Schottky Barrier in the source region since there is no barrier in drain region. Thus, S becomes a function of the gate capacitance, which is not expected, in a long channel MOSFET. In other way, to compensate for the impact of a ΔVds on the shape of the SB, gate voltage has to be adjusted by a ΔVgs through the coupling gate field to the SB.

IV.3.3. Experimental and Theoretical I-V curves:

Another point that may be interesting to do is to fit the experimental I-V curve with a theoretical one. Current flowing through a metal-semiconductor junction is composed of a thermionic emission and a tunneling emission. In most of the Schottky diode, the main mechanism is the thermionic mechanism. However, in our case, the source Schottky is reversed-biased, which is the contrary of the forward bias used in most diodes. That is to say, the current flows from the metal to the semiconductor. If we rely on the transport mechanism only on the thermionic emission, we may expect a saturation current density for the reverse bias. If we take into account only this mechanism, the theoretical curve would not fit the experimental curve. The tunneling should be taken into account; this may allow us to get a suitable theoretical curve that may fit to the experimental curve. By applying the 1D metal semiconductor transport theory [40], we will get the following expression:

$$J_{MS} = A^* T^2 \exp(-\frac{q(\phi_{Bp} - \Delta\phi)}{k_b T})\left[1 - \exp(-\frac{q|V|}{k_b T})\right] + \frac{A^* T}{k_b} \int_0^{q(V_b - \Delta\phi)} F_M(V) T(\eta)(1 - F_S) d\eta \quad \textbf{(IV-7)}$$

Here, A* is the Richardson constant, T is the absolute temperature, and kb is the Boltzman constant. Q is the charge, ϕ_{Bp} is Schottky barrier height for the metal and p-type semiconductor, and $\Delta\phi$ is the image potential lowering. The first part of the current density is related to the thermionic emission. The tunneling current is the second part of the above equation. $F_M(v)$ and $F_S(v)$ are the Fermi-Dirac distribution function of carriers respectively in metal and semiconductor, which has the following form:

$$F(V) = \frac{1}{\exp(\frac{\mu_i - qV}{k_B T}) - 1} \quad \textbf{(IV-8)}$$

where μ_i is the Fermi energy. The transmission probability, $T(\eta)$, is derived using the WKB approximation:

$$T(\eta) = \exp\left\{-\frac{1}{E_0}\left[\sqrt{qV_b}\sqrt{\eta + q\Delta\phi} - (qV_b - \eta - q\Delta\phi)\ln\frac{\sqrt{qV_b - \eta - q\Delta\phi}}{\sqrt{qV_b} - \sqrt{\eta + q\Delta\phi}}\right]\right\} \quad \textbf{(IV-9)}$$

where $E_0 \equiv q\hbar\sqrt{\frac{Nd}{4m\varepsilon s}}$

Here h is the Planck constant, ε_s is the dielectric constant of the semiconductor, m* is the effective mass, and Nd is the dopant concentration. η is the energy measured from the top of the barrier. On this basis, we could fit the experimental curve with theoretical curve. The fitted curves may included both the thermionic emissions and tunneling emissions. We may expect in this device that the tunneling is the dominant transport.

At this step, we can infer some properties concerning the transport that may be expected in our future experiment. Indeed, we could expect a current that is based on the tunneling through the source Schottky barrier. Thus, at Vds constant, an increase of Vgs results in an exponential increase of Id. This can be explained by the tunneling through source SD.

What can be infered is that the nanowires may work similar to a conventional MOSFET but physics are different. The role of the bulk maretial is minor; the main function of the tube is to provide SB at the source and the drain of Nano-FET.
Consequently, the linear region cannot be used to extract information about intrinsic properties. The shape is the response of the S/D SB to gate and S/D fields.

IV.3.4. Analogy with some other devices:

Some previous reports have already presented nanowires-FET. The results have been shown in the previous part.

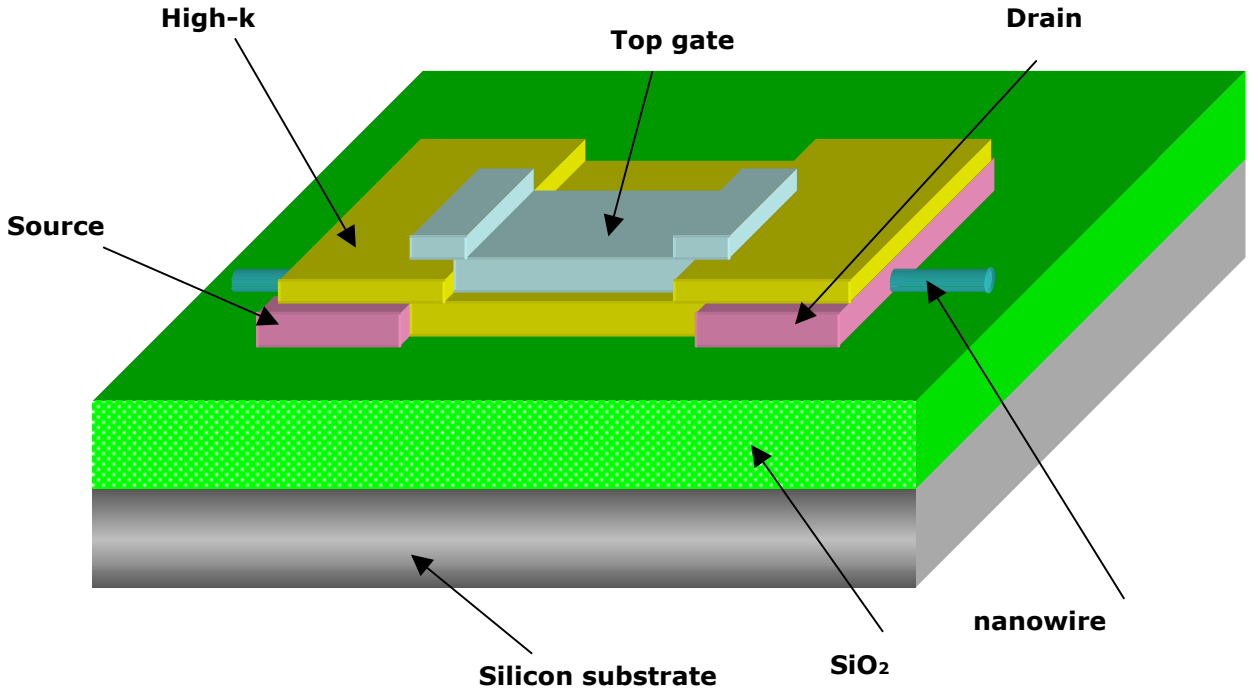


Figure IV-5: Scheme of a nanowires-FET.

We can see that this device is combination of many different breakthroughs:

- Silicon On Insulator
- Ultra Thin Body
- Metal Gate
- High-K dielectrics

We will explain briefly why these breakthroughs take place in this device.

As for Silicon On Insulator, the main advantage of this scheme is to confine the current through the nanowires to take the benefits of the quantum confinement in 1 direction.

Concerning the Ultra Thin Body, the diameter of nanowires (<10nm) would ensure a good electrostatic control of the channel in the "off" state.

As for the metal gate, this is related to the Source/Drain engineering. In this case, the use of metallic source/drain electrodes minimizes parasitic series resistance and eliminates the need of ultra shallow junction.

Eventually, the use of high-k is required to reduce the gate leakage by increasing the physical thickness and sustaining a low Equivalent Oxide Thickness.

Previously, we have answered to the question: what can we expect from the physical behavior of this new devices? We have seen that we may expect a physical behavior essentially due to the Schottky contact between Source and nanowires.

In the following part, we will focus our attention on the electrical results obtained by other groups. We will basically address an issue of the electrical benefits of this new structure.

IV.4. Interesting devices:

Nanowires have already been put in transistor that revealed pretty interesting electrical properties similar to the state-of-the-art of MOS devices without optimization. In this way, we can quote three interesting reports that have built this transistor. First, Ge nanowires FET [33], Si nanowires FET [31] have been implemented. I intend to describe these.

IV.4.1. Ge nanowires FET [33]:

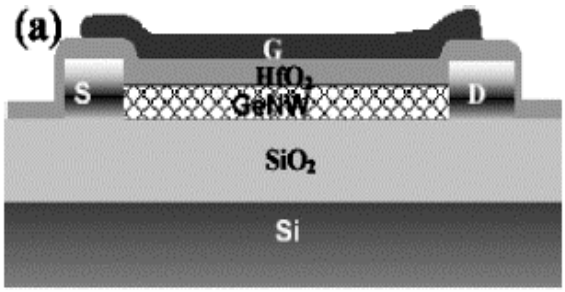


Figure IV-6: Ge nanowires-FET

In this device, it comes B-Doped with top gate structure, high-k into nanowires. It was reported in 2003 by Dai's group [33]. This device was built using the VLS method to synthesize the Ge nanowires. First, they used back gate configuration, with SiO2 as gate dielectric and Pd as the S/D contact metal. The S/D distances are L=5 μm. The second consisted of a top gate and 12nm high-k gate insulator grown by ALD and Ti/W were used as S and D electrodes, the Source/Drain distance in this case is 3 μm.

The electrical results reported by Dai are retrieved in the following chart:

Ge Nanowires FET type	Back gate	Top Gate
Ion/Ioff ratio	10^3	10^3
Transconductance	0.21 μS	0.21 μS
Current per nanowire	3 μA	3 μA
Subthreshold slope	300 mV/decade	750mV/decade
Hole mobility	600 cm^2/Vs	200 cm^2/Vs

Table IV-1: Electrical data of Ge-Nanowires FET.

What we can notice from these results is the interesting hole mobility which is close to the highest hole mobility got up to now (700 $cm^2V^{-1}s^{-1}$), this points out the high quality of the nanowires grown by VLS method. We have to notice that these devices have not been passivated, consequently, the other result may be attributed to the interface states between Ge nanowires and SiO2 or in the case of the top gate device, and it may be

due to the interface between the HfO_2 and the Ge nanowires. However, the top gate structure unveils promising characteristics and the performance is at least comparable to that of Ge MOSFET with HfO2 gate insulators fabricated on Ge wafers and this without any optimization. [41]

IV.4.2. Silicon nanowires-FET [31]:

In our case, the most interesting report is the one concerning the high performance silicon nanowire field effect transistors written by Lieber's group [31]. The reported device is a back gate structure; source and drain were defined by electron beam lithography and subsequent evaporation of 50 nm Ti and 50nm Au.

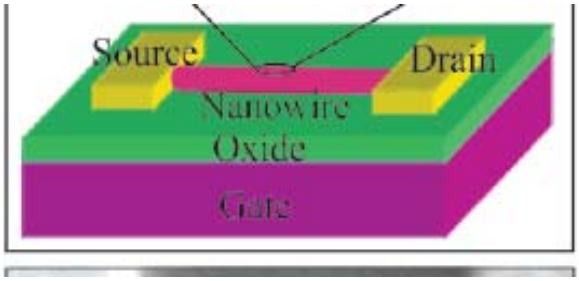


Figure IV-7: Silicon nanowires

Results are sum-up in the following chart:

Si Nanowires FET type	Back gate
Ion/Ioff ratio	10^4
Transconductance	17-100 $\mu S / \mu m$
Current per nanowire	50-200 $\mu A / \mu m$
Subthreshold slope	174-609 mV/decade
Hole mobility	230-1350 cm^2 / Vs

Table IV-2: Electrical data of Si-nanowires FET.

These results have been converted to the length of the state-of-the-art planar Si device. This conversion relies on the following assumptions:

- The capacitance is based on the cylinder model that is based on the infinite plate model.
- Do not take into account for the interface trap states that may affect the transconductance.

These are the results:

SI Nanowires FET type	Nanowire Converted data	Planar Si device
Gate length	50 nm	50nm
Gate oxide thickness	1.5nm	1.5nm
Mobility (cm^2/Vs)	230-1350	
Ion ($\mu A/\mu m$)	2000-5600	650
Ioff ($\mu A/\mu m$)	4-45	9
Subthreshold slope (mV/decade)	60	70
Transconductance ($\mu S/\mu m$)	2700-7500	650
Hole mobility	$600\,cm^2/Vs$	$200\,cm^2/Vs$

Table IV-3: Electrical data, comparison.

What we can notice from these results, is the amazing value of the mobility. Indeed, the highest and the average hole mobility values of 1350 and 560 cm^2/Vs in p-Si NWs are more than an order of magnitude larger than the value in the bulk, 40 cm^2/Vs. From this report, Lieber'group operated a surface passivations and source-drain contact thermal annealing which were found to significantly improve the FET performance. For example, we can note the increase of the average transconductance from 45 to $800\,nS$ and the mobility from 30 to $560\,cm^2/Vs$. Finally, the comparison between the converted data of the nanowires-FET and the state-of-the-art planar Si device showed that this device have the potential to substantially exceed conventional devices.

Now, let's discuss the electrical performances to enhance the motivation concerning this project. Through the two previous reports, these new devices have

demonstrated interesting electrical performance. Even without optimization, the GE-nanowires-FET demonstrated electrical results which are similar to the conventional MOSFET. As for the silicon nanowires FET, the converted data demonstrated that this device is suitable for the future development of the nanoelectronics. Thus, thanks to the high value of hole mobility, this device may be suitable to the high-speed device. The improvement of the transconductance allows us to get a better voltage gain.

Up to now, we have discussed about the electrical performance of nanowires MOSFET. The question now is how to build this device.

IV.5. How to build a nanowires-FET:

In this part, we will discuss about the different ways to build the nanowires-FET. So, first we will describe the different ways to prepare the substrate. Then, we will focus on the different way to deposit nanowires.

IV.5.1. Preview of our future device:

Before beginning, let's we introduce the device we would like to build in SNDL laboratory:

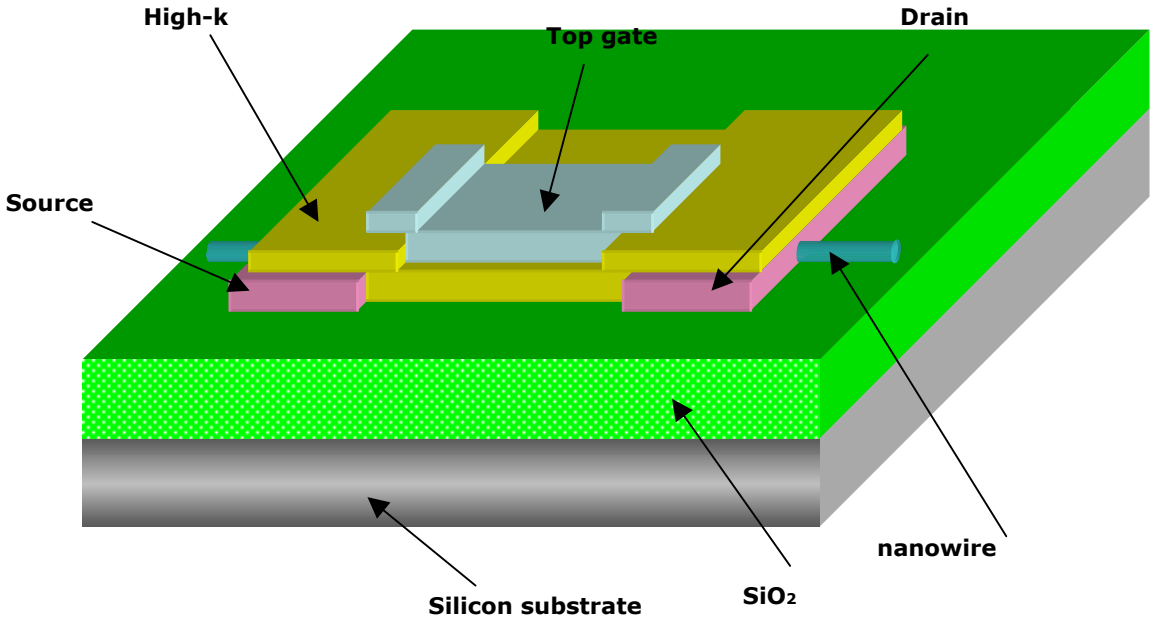


Figure IV-8: Scheme of our device.

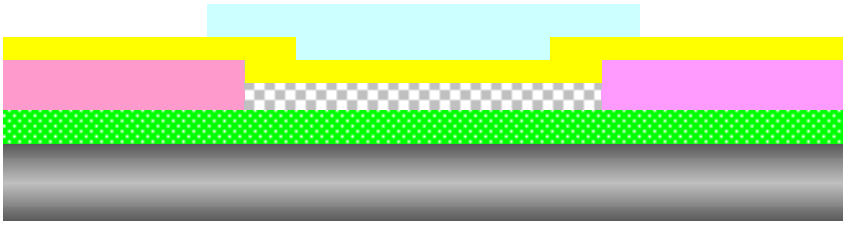


Figure IV-9: Cross section of our device.

Above, this is a cross section view and a global view of our nanowires-FET. It consists of an oxide layer SiO2 above a silicon substrate, nanowires deposited on the oxide layer, metal source/drain, high-k dielectric and a metal gate.

Indeed, the process to build a nanowire is divided into three main steps. First, the growth of Silicon nanowires using the VLS method, the “nanowires deposition” process and then the normal process flow.

IV.5.2. Vapor-Liquid-Solid:

Indeed, the VLS method requires a particular substrate. The substrate needs to be prepared before operating the growth of nanowires. Indeed, we cannot just deposit the gold colloidal solution on the wafer, otherwise the gold colloidal will form some clusters and thus prevent us to get small diameter nanowire [42].

IV.5.2.1. Preparation of the substrate:

Indeed this step is to place the gold particles on the substrate and prevent them from form some clusters. This is realized by using the hydrophilicity and hydrophobicity [43]. The scheme of the process is described below:

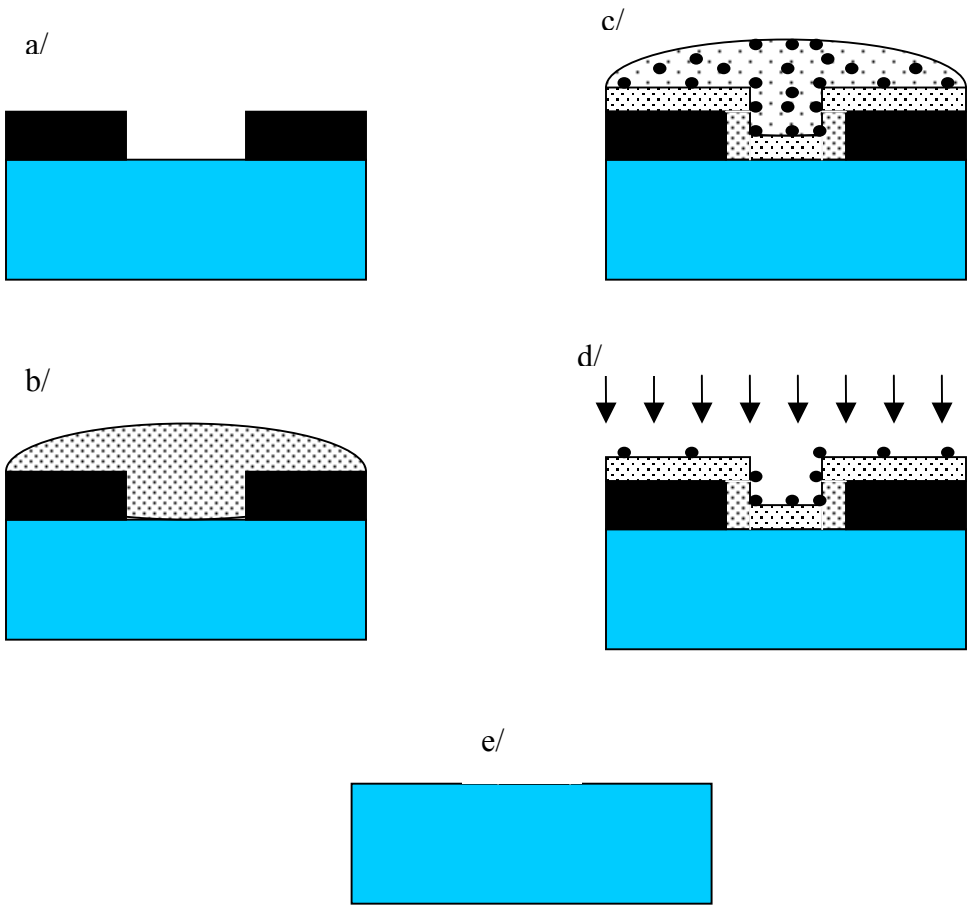


Figure IV-10: Deposition of gold colloids.

These are the different steps to deposit the gold particles:

- a/ the resist developed to form desired patern
- b/ poly-L-lysine added to the structure
- c/ poly-L-lysine washed from the surface and colloidal solution applied
- d/ the substrate comprising resist and gold colloids which are dry
- e/ final structure with gold colloid island.

This is the sequence we should use to deposit the nanoparticles on our substrate:

Patterned adhesion of colloids using poly-L-lysine:

Poly-l-lysine solution (0.1% aqueous solution, P8920, SIGMA, UK) is applied to the patterned resist surface resulting in an adhesive surface where the resist has been removed, and also on the remaining resist. 100 microliter per centimeter square is left for 1h to react with the surface. Then RO water was pipetted directly onto the surface to rinse it. Having undergone the poly-L-lysine treatment, substrates are immersed in a gold colloidal solution (Ted Pella, ref:15702-5) for 1 h. Following the immersion in the solution, structures were dried with a nitrogen gun held perpendicularly to the surface, in an attempt to limit capillary effects altering colloidal packing. It is important for the nitrogen to hit the surface at 90degree, as this reduces the movement of both poly-L-lysine and gold colloids from their original position.

Removing the remaining resist:

Considering a positive resist (Chestec, UK), samples are placed in a beaker of acetone and put in a sonicator for 5 min. The acetone is poured off and samples were placed under a continuous flow of RO water for 3 min prior to being dried with nitrogen gun.

Indeed, another method would be the following based on the APTS (Aldricht): Oxide silicon is cleaned in acetone and ethanol and then immersed into a Piranha solution. Then, the substrate is exposed to UV-ozone and rinsed with DI water. A 100 nm thick PMMA resist layer was spun onto the cleaned susbtrate and patterned. To improve the reactivity of the patterned surface and remove any organic contaminants from the substrate, it was cleaned with oxygen plasma. Then, a layer of APTS was deposited by CVD and consequently, the sample was allowed to react with gold colloid solution. Finally, the PMMA layer was lifted off in acetone.

To explain this, there are two phenomena we have to take into account. The first one is the reaction between the hydrophilicity of the silanol groups of the oxide surface and the hydrophilic part of the chemical reactant. This is called the silanization chemistry which is performed to deposit monolayer coverage via organosilane reactions with hydroxyl groups on the silica surface, producing layer with known terminal groups.
Then, the next phenomenon is related on the electrostatic anchoring of surfactant covered gold particle on amino-silane functionalized surfaces.
To improve this phenomenon, we have to use a wet chemical grown oxide. They are hydrophilic in contrast to thermal oxides. These oxides are generally covered with surface hydroxyl groups (Si-OH) called silanol groups, and are very similar in their behavior with respect to silica gels, which are used for metal adsorption, as a substrate for catalysts, and for other applications [44]. Geometrical considerations and chemical

measurements indicate an average surface density of around five (typical range 2-12) hydroxyl groups per nm^2 [45].

What can be infered is that the hydroxyl group density will not limit the density of gold colloid particle since the diameter of these gold particles is about 5nm.

Following this step, the prepared substrate is placed in a furnace to operate the VLS method. Below are different recipes used by different groups:

IV.5.2.2. Substrate preparation and CVD growth [46]

A Si substrate with a thermally grown oxide layer (500 nm thickness) was cleaned with acetone, methanol, and isopropanol. It was then dipped into a solution of 3-aminopropyltriethoxysilane (APTES, 12 mL in 20mL H2O) for 30 minutes, rinsed with deionized water and blow-dried. The substrate was soaked in an aqueous Au colloid solution (20 nm diameter, Alfa Aesar) for 1 h. The APTES monolayer renders the SiO2 surface positively charged and allows for the deposition of Au colloids (negatively charged) with high efficiency. For CVD, the substrate was placed at the center of a 2.5 cm quartz-tube reactor within a furnace. The reactor was heated to 275C under a H2 flow of 110 sccm. The gas flow was then switched to 10 sccm of GeH4 (10% in He, Voltaix, NJ) and 100 sccm of H2 (99.99%, Praxair, CA) for 15 min before switching the gas back to H2 only, and cooling the system to room temperature.

Comments: desired nanowires growth results are got by controlling the GeH4 decomposition through H2 addition:

GeH4 → GeH2 + H2 activation energy: 50kcal /mol

GeH2 → Ge + H2 activation energy: 35kcal /mol

With a flow of H2 50sccm, during CVD under constant GeH4 flow (10sccm, 10% in He) at 275C, there is an excessive GeH4 pyrolysis with H2 flow rate below 50sccm. The consequences are significant amorphous coatings on the substrate and reactor wall. Above 200sccm, the substrate and CVD wall were clean. The pressure in the furnace reactor is 1 atm. To better understand this effect, refer to the paragraph III.B.3.c.

IV.5.2.3. Silicon Nanowires [47]:

The as-made Au clusters were dispersed in a precursor solution for synthesizing mesoporous silica. The precursor solution consists of (molar ratio) 0.01 poly(ethyleneoxide)-*b*-poly(propyleneoxide)-*b*-poly(ethyleneoxide) (EO20-PO70EO20):1 tetraethoxysilane:40 ethanol:0.02 HCl:8 H2O [48]. A thin film was deposited on a Si wafer using spin coating. The sample was then calcined at 600 °C for 5 h, resulting in a thin mesoporous film embedded with uniform Au clusters. The substrate was then used to grow Si nanowires in a home-built CVD system. Briefly, SiCl4/H2 gas precursors with flow rate of 400 sccm were introduced into a tube reactor at reaction temperature of 965 °C. The growth generally takes 1.5 min.

IV.5.2.4. Ge & Si nanowires [49]:

Gold nanoclusters were deposited on oxidized silicon wafers and placed in a quartz tube furnace. Silicon nanowire cores were grown at 450C using silane ($5\,cm^3$ at standard temperature and pressure, STP/min) at 5torr, producing a one-dimensional (axial) growth rate of about $2\mu m/\min$. p-type silicon shells were deposited using silane ($1\,cm^3$ STP/min) and 100 p.p.m. diborane in helium (20 cm^3 STP/min) at 20 torr yielding a

radial growth rate of about 10 nm/min, stoechiometry incorporation of boron would yield a bulk doping level of $2.10^{20} cm^{-3}$, and is similar to the values obtained from transport measurements. Ge nanowires were grown at 380C using 10% germane in argon (30 cm^3 STP/min) at 30 torr (axial growth rate, $0.2 \mu m / \min$), while Ge shells were deposited at 5 cm^3 STP/min and 4 torr (radial growth rate, 10nm/min) by changing the position of the growth substrate within the furnace. The amount of reactant that has thermally decomposed typically increases as the gas flows through the furnace, and thus radial growth may be 'turned on' by moving the growth substrate downstream to favour uncatalysed surface growth. Oxidation of i-Si cores to interrupt epitaxy was accomplished by flowing oxygen (30 cm^3 STP/min) at 30 torr for 2min. The oxide gate dielectric in the coaxially gated structures was grown at 450C using oxygen (2.5 cm^3 STP/min) and silane (0.25 cm^3 STP/min) at 1 torr for 2 min.

From these recipes, we can extract the following information concerning the condition we have to settle:

We can notice through these reports that the choice of this group highlighted what we have deduced from the impact of the different parameters. Thus, the low pressure is chose to get an axial growth rather than a radial growth which is improved by increasing the pressure of the materials.

As for the flow, a small flow is required to reduce the axial growth. This phenomenon can be understood by the following steps: with a small gas velocity, the Reynolds number is reduced, consequently, the diffusion of materials through the boundary layer is reduced, so in that case the axial growth is not favored since the amount of material is reduced. Consequently, these two effects will favor uncatalysed surface growth.

IV.5.3. Eutectic point:

Another question that can be raised is the eutectic temperature used in the experiment and those quoted from the theory. The temperature is much lower than this predicted by the theory. This can be explained by the fact that the phase diagram doesn't take into account the size of the particle. We will try to explain this difference with the following assumption: the nanoparticle consists of only one material and is not covered by stabilizator as it is in the colloidal solution [50].

To understand the root of the properties of nanoparticle, the simplest way is to examine how their size and their shape affect these properties. The top-down approach has been already used, that is to say to start from the bulk material and go the nanoparticle. This allows us to use the thermodynamic. Consequently, this analysis allows us to highlight the variation of phase diagram with the size, the shape and defects of nanoparticles.

Let's describe the thermodynamic of the nanoparticles. It relies on the evaluation of the free energy, G(T). If we take N as the number of atoms in the particle, to apply the thermodynamical theory, N has to be high. We suppose that the particle surface is characterized with one tension superficial. To a given temperature, the free energy of Gibbs is given by the following equation:

$$NG = NG_{\infty} + fN^{2/3}\gamma \quad \textbf{(IV-10)}$$

Where f is a geometrical term depending on the shape of the particle. The term $(fN^{2/3})$ is equal to the number of atoms at the surface. γ is the superficial tension per atom, that is to say the superficial tension divided by the numbers of atoms at the surface. For most of the inorganic materials, γ is independent on the temperature, T.

G_∞ and G are respectively the energy of volume per atom of the bulk material and of the particle, in a given phase.

The stability of one phase compared to another results from the minimization of the free energy between phases. Take $G_i, G_{i\infty}, \gamma_i$ which are the free energy per atom in the particle, in volume and the superficial tension in the phase i. The equilibrium between phases obeys the following equation:

$$N(G_1 - G_2) = N(G_{1\infty} - G_{2\infty}) + fN^{2/3}(\gamma_1 - \gamma_2) \quad \textbf{(IV-11)}$$

The transition takes place when (G1-G2)=0. The phase 1 is the thermodynamically stable phase when (G1-G2)<0. When we take into account the surface term, we highlight that the temperature transition of nanoparticle is not the same one as in volume. It depends on the size of the particle.

Among the transition phase, let's consider the fusion temperature. The fusion temperature Tm is much higher than the solid Debye temperature in inorganic solid. So, the calorific capacity of the solid is nearly constant and,

$$G_{1\infty} - G_{c\infty} = C - BT \quad \textbf{(IV-12)}$$

Where C and B are constant for a given solid. The index 1 and c are related to the liquid and solid phase respectively.

In solid inorganic material, γ is nearly independent on the temperature. Thus, the fusion temperature of the nanoparticle will modify with the radius R, as:

$$T_m = T_{m\infty} + f(\gamma_1 - \gamma_c)/BN^{1/3} = T_{m\infty}[1 - \alpha/(2R)] \quad \textbf{(IV-13)}$$

Where $T_{m\infty}$ is the usual fusion temperature. The linear relation has been demonstrated experimentally in metal and semiconductor. The inorganic materials are characterized by a positive α, between 0.4 and 3.3 nm.

Some expressions concerning the parameter α have been proposed. The most famous one was revealed by Palow (1909) and modified by Hanszen (1960):

$$\alpha = 4V_s[\gamma_{sv} - \gamma_{lv}(\rho_s / \rho_l)^{2/3}]/(H_m R) \quad \textbf{(IV-14)}$$

Where Vs is the molar volume of crystal, γ and ρ are respectively the interfacial energy per unit area and mass per unit volume, the indexes s, and v are the solid, liquid and vapor phase, Hm is the molar enthalpy of fusion.

For most of cubic metal, $\gamma_{sv} - \gamma_{lv} \approx \gamma_{sl}$, and $\rho_s = \rho_l$. Thus:

$$\alpha = 4V_s\gamma_{sl}/(H_m R) \quad \textbf{(IV-15)}$$

Introducing this relation in the equation, we can find the Gibbs-Thomson equation. For reference, α is equal to 1.27 nm for Ag. In the previous equation, we can note the role of the interfacial tension. So, when the nanoparticle is shielded with a layer whose material is different from the one in the core or when the particle is closed in a matrix, the interfacial tension is different from the free particle. In that case, the variation of Tm with R is less important than for a free particle.

IV.5.4. Deposition:

After growing the nanowires, a choice has to be made: either to pick nanowires up from the substrate, either to use the same substrate to build the device. We will discuss the different ways to do the "deposition". Indeed, the major drawback is to align nanowires. First, we will discuss the different ways to align nanowires on the same substrate where they have been grown so called Self Assembly Process. Then, we will discuss the way in which we remove nanowires from the substrate. To better understand, let's sum up the different ways in a chart:

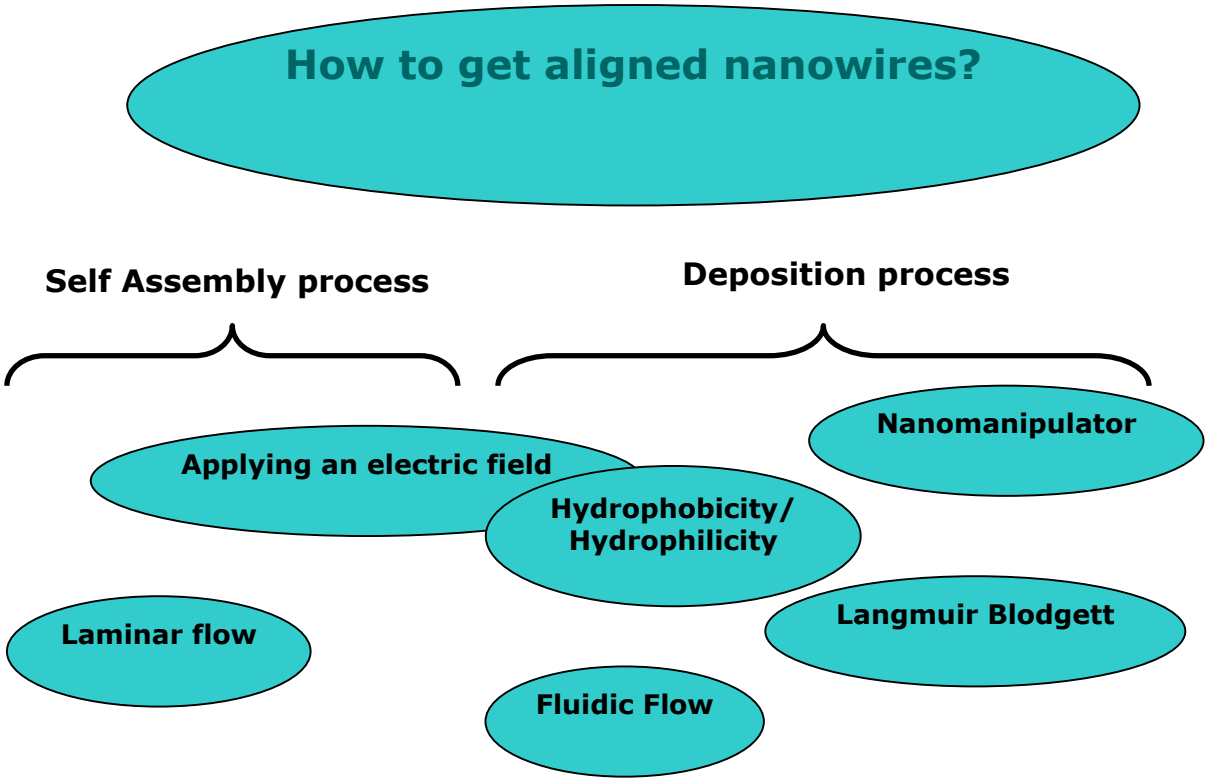


Figure IV-11: diagram of the different way to get align nanowires.

We will review the different process already used by other groups. Then we will discuss about the ability of other process and propose a suitable process to use in the future to evaluate reliability of such a device.

First, concerning the alignment process in self-assembly process, we can quote the use of applying electric field and the use of laminar flow to align nanowires during their growth.

IV.5.4.1. Applying an electric field:

The purpose of this method is to grow Silicon nanowires onto the surfaces of SiO2 substrate within established electric fields across patterned metal gate [51], [52]. That is to say to apply an E-field via Cathode/anode on the substrate to align them.

Indeed, without any electric field, the nanowires grow randomly. During the growth, nanowires are aligned.

In a simple way, we could think that applying an electric field will allow us to align nanowires. Nevertheless, this mechanism is composed of two mechanisms; the first one is the electric field distribution and the Van der Walls interaction between the nanowires and the substrate.

The first consideration is the electric field. It could damage the substrate, even if it is used to align the nanowires, that is to say, to use the electric field which is parallel to the substrate, the applied voltage will induce an electric field which is perpendicular to the substrate and may induce an electrical breakdown. To give an idea, the electrical breakdown of the SiO2 are: $>10^7$ V/cm in thermal oxides; can be as low as 10^6 V/cm in CVD oxides. As for a 500nm oxide layer, the maximum voltage we could apply would be at rough estimate at 500V. And some previous report concerning the nanotubes, some good results have been achieved with voltage up to 20 V across a gap of 10 μm between the two electrodes where nanotubes have been set. In the case of nanowires, the tip of the nanowires may enhance this phenomenon due to its polarity. Even if its ability has been demonstrated, this method is not reliable for two reasons, the induced damages by the electric field as discussed above and the interaction of Van der Walls with the substrates.

This electric field has to overcome the Van der Walls interaction between the nanowires and the surfaces. Let's briefly describe this interaction:

Indeed, at this scale, we have not only the usual inter-atomic interaction but the Van der walls interaction as well. Actually, the main forces responsible for adhesion are the Van der Walls forces. The Van der Walls interaction inter-atomic potential are given by:

$\varepsilon = -C/r^6$ **(IV-16)**

where C is a positive constant and r is the inter-atomic distance.

For instance, the interaction between two plates, separated with a distance x, is obtained by the sum over all the interaction atom-atom:

$\varepsilon_{plate-plate} = -\pi n^2 C/12x^2 = -H/12\pi x^2$ **(IV-17)**

where n is the atomic concentration and H is the Hamaker constant. For solid, H is about 10^{-19} J in the air.

The attraction force between two plates is given by the derivation of the $\varepsilon_{plat-plate}$ with respect to x, so:

$F(x) = H/6\pi x^3$ **(IV-18)**

The shape of the above equation depends on the shape of the two objects in interaction. The interaction between two solids is observed when the distance is lower than 10nm. Below is a table presenting some van der Walls interaction:

Object	Interaction of Van der Waals
Two infinite plates	$-H/12\pi x^2$
Two plates of thickness d separated with a distance x	$-(H/12\pi)[x^{-2} + (x+2d)^{-2} - 2(x+d)^{-2}]$
Two spheres of radius r, whose distances between them are R=sr	$-(H/6)[2(s^2-4)^{-1} + 2s^{-2} + \ln(s^2-4) - \ln(s^2)]$

Table IV-4: Van Der Waals interaction.

Just to get an idea, let's consider the order of magnitude of these two forces:

- Electric field: F= $L^2 E_{Field}$
- Van der Waals: F=H L^{-3}

Let's consider some value, L~nm, Efiel~V/μm, H~10^{-19} J. After a short evaluation, we could deduce that the Van der Waals interaction is some orders higher than the electric

field applied. So, the electric field has to overcome this interaction without damaging the substrate.

IV.5.4.2. Laminar flow:

Another approach would be the use of laminar flow to align nanowires during their growth. Some reports have unveiled the inefficiency of using the laminar flow. A calculus was performed and the result given revealed that the force due the laminar flow force was seven orders less important that the one applied with an electric field. However, the result is not really accurate since they used in the report the gas velocity. Indeed, at this scale, due to the boundary condition, the gas velocity is much less important than the selected one. Consequently, relying on the following equation:

$$F = (mP / RT)ldv^2$$

the force due to the laminar flow is all the more inefficient as we take into account the boundary condition. To better understand this phenomenon, we can rely on the figure III.2.

Above were the two ways of getting aligned nanowires known up to now, we have seen that these were not really reliable. By the way, these are not exhaustive, and some other ways can also be used.

Let's discuss the process deposition in which nanowires are grown and subsequently, picked up and aligned on other substrate. In this section, we will cover the fluidic flow, the Langmuir-Blodgett method. We will introduce briefly the nanomanipulator and then propose a way to deposit nanowires aligned.

To better understand the process deposition, let's us describe briefly. After the growth, the nanomaterials are then harvested by placing them in a liquid solvent (such as ethanol)

and blasting them with ultrasonic waves to loosen them from the wafer surface. Then, they are deposited either all over the wafer like the Langmuir-Blodgett method or on specific location like the fluidic flow.

IV.5.4.3. Fluidic flow method:

Lieber's group managed to align nanowires through this method in Directed Assembly of one Dimensional Nanostructures into functional networks [53]. In this report, the materials have been put into ethanol solution and then passed suspensions of the nanowires through the fluidic channel structures from between a poly-dimethylsiloxane (PDMS) mold and a flat substrate (figure IV.13). The average nanowires space in the thin film was controlled by varying the NW concentration in the solution and the total flow time. With this approach, the alignment can be extended over large area by using longer flow channel mold. Still the average space between nanowires is relatively high, at about 100nm. So even if we get aligned nanowires, this method doesn't allow to set precisely nanowires at the desired location. Compared to the electric field method, the fluidic flow doesn't require an extensive lithography to fabricate the electrodes for assembly.

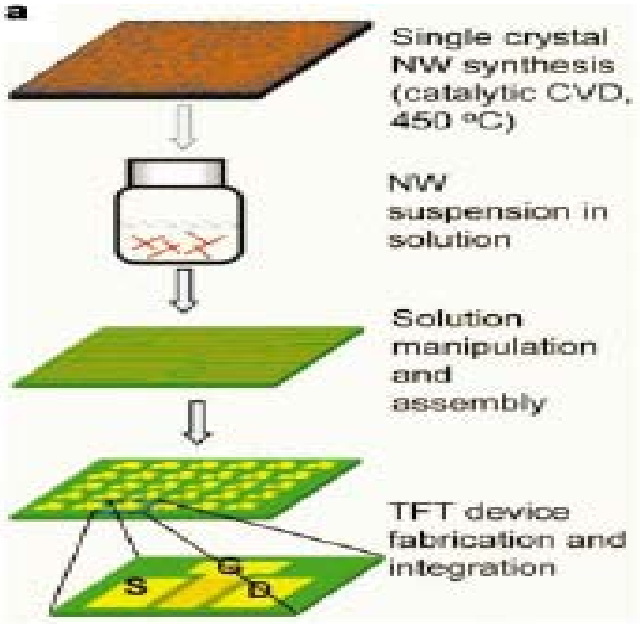


Figure IV-12: illustration of the deposition process [36].

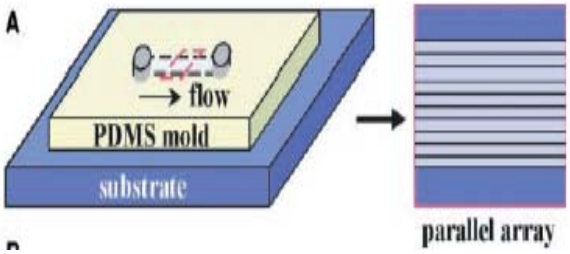


Figure IV-13: Illustration of the PDMS process [53].

IV.5.4.4. Langmuir-Blodgett

Another approach which seems to be more interesting than the previous one, the Langmuir-Blodgett is one of the most promising techniques for getting such an array of parallel nanowires [54] (figure IV.12). It enables a homogeneous deposition of monolayer over a large area and a possibility to make multilayer structures. Briefly, it consists in spreading amphiphilic molecules on a water surface. It forms monolayers or films where the hydrophobic segments stem at the water/air interface. The molecules can

be compressed to give monolayers with controlled density and organization. Then, Langmuir-Blodgett films are obtained from the deposition of monolayers on a solid substrate.

Let's describe the process; many groups have managed to get aligned nanowires through this method. [55] They reported a close-packed nanowires as parallel arrays, with their longitudinal axes aligned perpendicular to the compression direction. To better understand this phenomenon, and to know what the requirements are to set up this process in this lab, we will discuss about the theory underlying this method.

The nanowires, in this case Silicon nanowires have a SiO2 shell, consequently they have a hydrophilic surface to be functionalized with a surfactant. Indeed a surfactant is a larger class of molecules which consist of a hydrophilic (water soluble) and a hydrophobic (water insoluble) part. This amphiphilic nature of surfactants is responsible for their behavior in solution and their accumulation at the interface between air and water. Thus, the hydrophobic nature of Si-nanowire is functionalized with the hydrophobic part of the surfactant and thus let at the external shell the hydrophilic part of this molecule.

This amphiphilic molecule consists of a hydrophilic part which is generally a hydrocarbon chain and a hydrophobic part which is a polar group such as –OH, -COOH,-NH3+…).

The surfactant-nanowires are then deposited in the water trough of Langmuir-Blodgett tool and form a monolayer over the surface. At this step, the surface pressure is zero and nanowires are randomly dispersed on the surface. Indeed, when the available

area for the monolayer is large, the distance between adjacent molecules is large and their interactions are weak. Under these conditions, the monolayer has little effect on the surface tension of water.

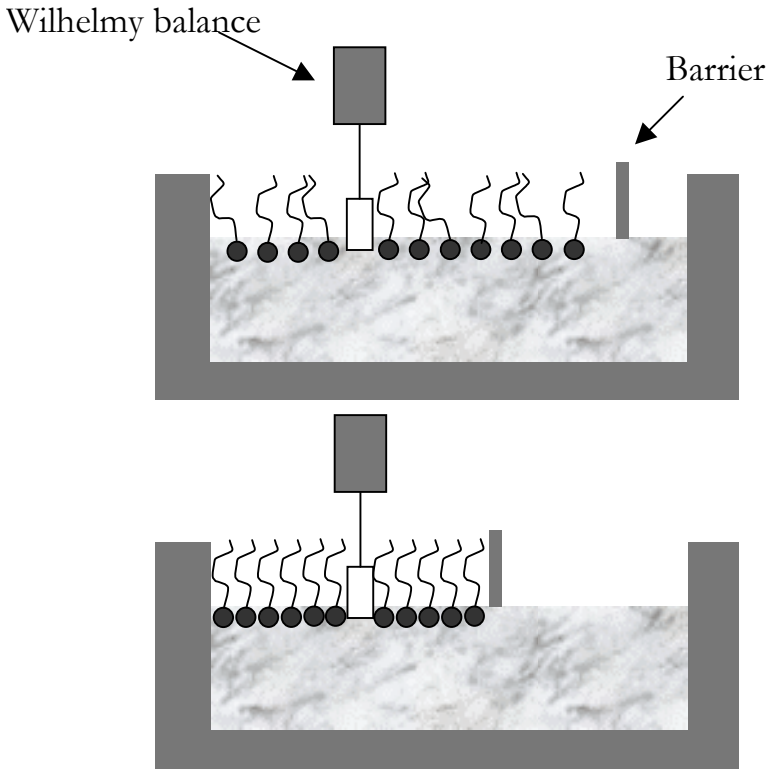


Figure IV-14: Langmuir Blodgett tool

Then, if the area is reduced by a system barrier (figure IV.14), the molecules start to exert a repulsive effect on each other. And the surface pressure will begin to increase as we can deduce form the following equation:

$$\Pi = \gamma - \gamma_o \quad \textbf{(IV-19)}$$

where γ is the surface tension without a monolayer and γ_o the surface tension with the monolayer. And this surface pressure is the most important means to control the properties of a monolayer. It consists in measuring the surface pressure as a function of

the area of water available for each molecule. Indeed, repeated experiments should be carried out to get a reproducible trace. Below is a scheme of this chart (figure IV.15):

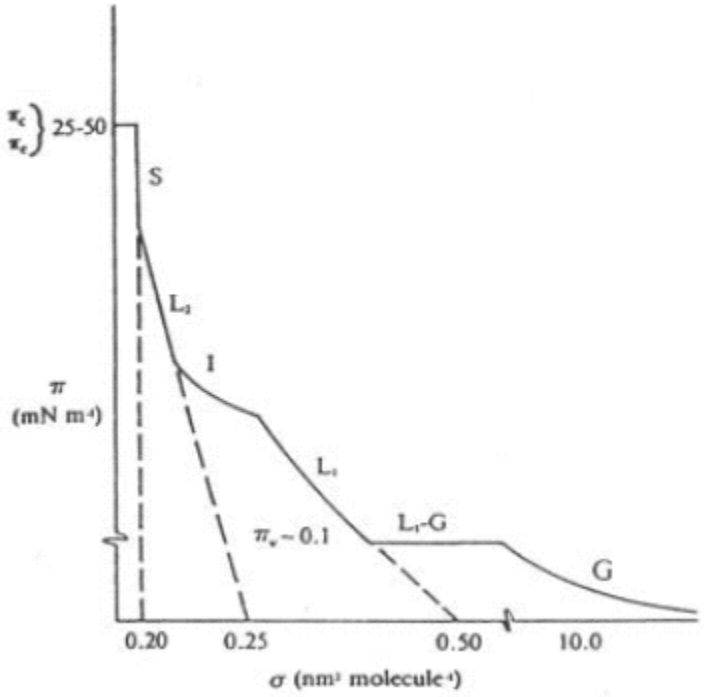


Figure IV-15: Isotherm Scheme [57].

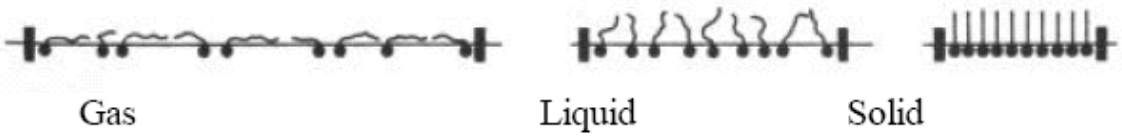


Figure IV-16: orientation of the molecules in different phase [58].

Indeed, a number of different regions come up on examining the graph. These different regions are called phases. When the monolayer is compressed, it passes through several phases which are identified as discontinuities in the graph. W.D Harkins proposed a terminology to classify different monolayer phases (figure IV.16). At zero compression the monolayers exist in the gaseous state and can, under compression, undergo a phase

transition to the liquid-expanded state. Further compressions the phase undergoes a transition to the liquid-condensed state and at even higher compression; the monolayer eventually reaches the solid state. Beyond two compression level, the monolayer will collapse characterized by a rapid decrease in the surface pressure.

So, at this step, under a certain pressure, the nanowires are aligned in the water trough of Langmuir Blodgett tool. For example, for Silicon nanowires functionalized with1-octadecylamine, the surface pressure required is 55-60mN/m. This pressure depends on many parameters such as the temperature, the physical and chemical properties of the hydrophobic and hydrophilic groups. That is why it would be required to repeat the process to get the surface pressure required to get the nanowires aligned.

Then once nanowires are aligned, they are deposited on a surface. This is done by dipping the solid substrate up and/or down through he monolayer while maintaining the surface pressure constant by a controlled feedback. Thus, the monolayer is deposited on the substrate. This layer is called Langmuir-Blodgett layer. The deposition process is described with the following pictures (figure IV.17):

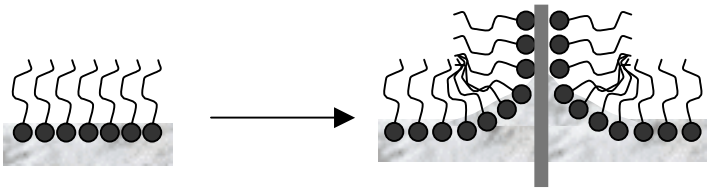


Figure IV-17: Langmuir blodgett layer for hydrophilic material.

Indeed, the surface should be kept high enough to ensure a good cohesion in the monolayer. The way of dipping the substrate depends on the chemistry of the solid. When

the solid substrate is hydrophilic (SiO2) the first layer is deposited by raising the solid from the subphase through the monolayer, whereas if the solid id hydrophobic (Si) the first layer is deposited by lowering the substrate into the subphase through the monolayer (figure IV.18).

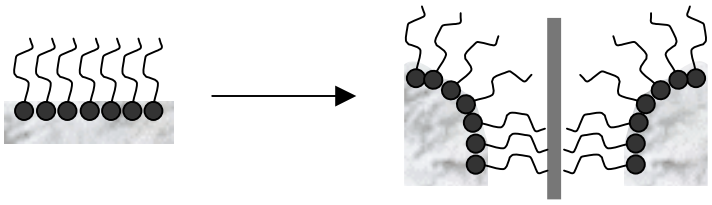


Figure IV-18: Langmuir Blodgett layer for hydrophobic material.

Let's describe the Langmuir-Blodgett tools. The Langmuir-Blodgett tool is composed of a trough which is thermostated by circulating water underneath it, barriers, and a hydrophilic material and is heavy enough to prevent any leakage of the monolayer beneath the barrier. The surface pressure is measured by the Wilhelmy plate-method.

With this method, the measurement is done by determining the force due to surface tension on a suspended plate. This force is converted into surface tension as follow (figure IV.19).

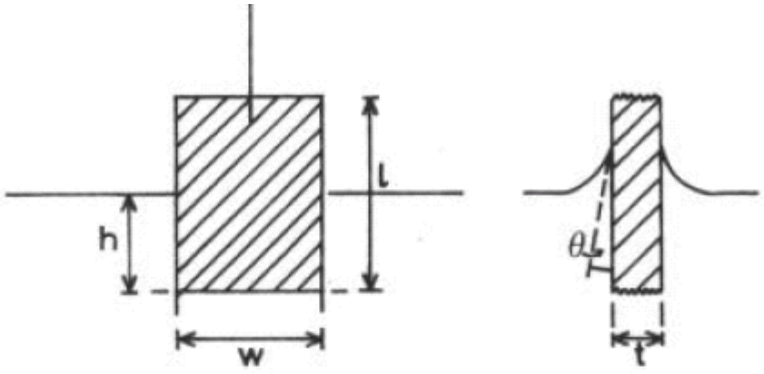


Figure IV-19: Wilhelmy plate partially immersed in a water surface [54]

The forces acting on the plate consist of the gravity and surface tension downward and buoyancy due to displaced water upward. For a rectangular plate of dimensions l, w and density p immersed to a depth H in a liquid density p_1, the downward force is given by the following equation:

$$F = \rho glwt + 2\gamma(tp)(\cos\theta) - \rho_1 g t_1 w_1 h_1 \quad \textbf{(IV-20)}$$

where γ is the liquid surface tension, θ is the contact angle of the liquid on the solid plate and g is the gravitational constant. The surface pressure is then determined by measuring the change in F for a stationary plate between a clean surface and the same surface with a monolayer present. For example with a plate completely immersed that is to say $\cos\theta$=1, the surface pressure is obtained form the following equation:

$$\Pi = -\Delta\gamma = -[\Delta F / 2(t + w)] = -\Delta F / 2w \quad \textbf{(IV-21) if the plate is very thin.}$$

This method may be really efficient in the project. It allows to get a large area covered with aligned nanowires. Consequently, we may apply a lithography process to remove nanowires from the undesired location over the wafer. Thus the normal process flow can follow.

IV.5.4.5. New approach:

Another approach may be used, it relies on the interaction between the hydrophobic part and hydrophilic part of surfactants. This can be used in our project without any added tools such as the Langmuir-Blodgett tools.

The process could be described as follow. A PMMA mask covered the SiO2 substrate, then the PMMA mask is defined by e-beam lithography; the substrate is silanized; then

nanowires covered with surfactants is deposited on the template. Then the mask is lifted-off, leaving the nanowires on the substrate.

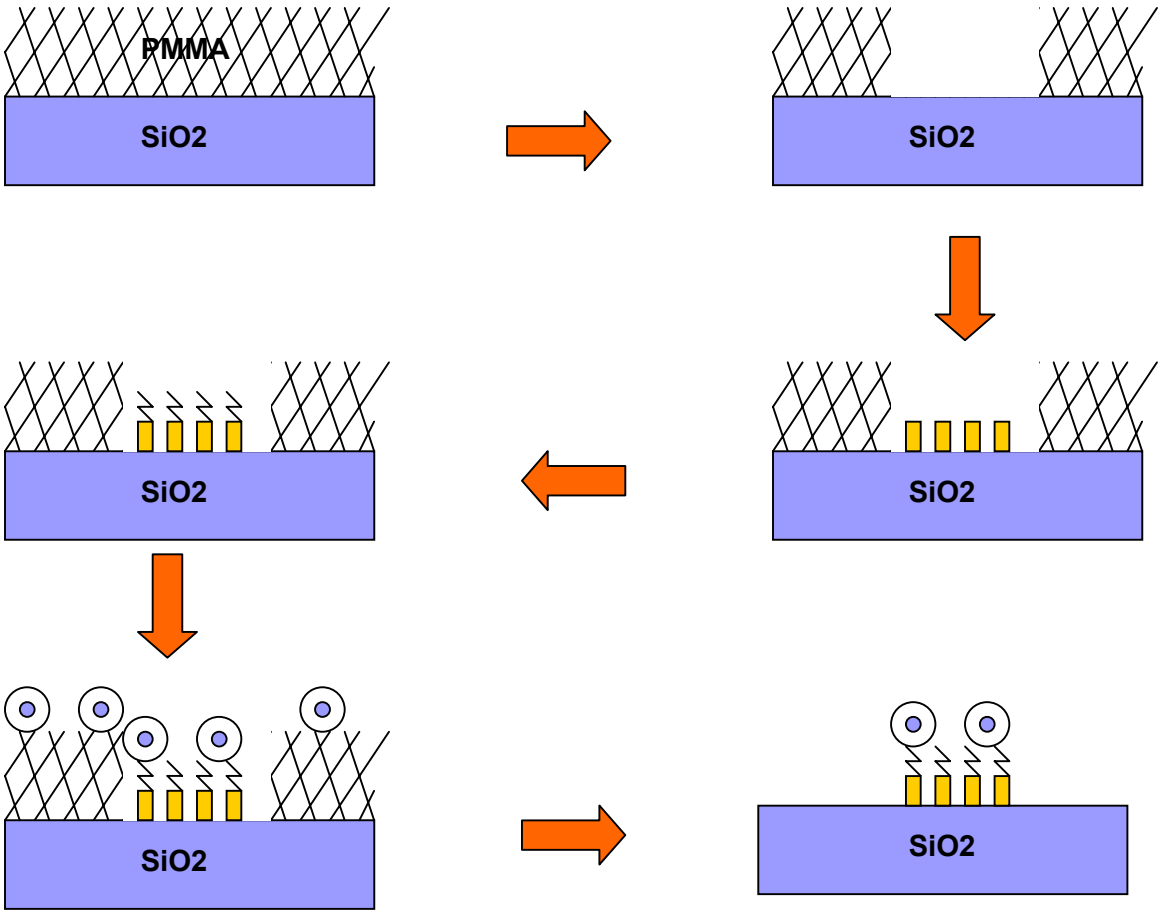


Figure IV-20: Illustration of the new deposition process.

This method may be suitable to contact NWs with metallic electrode in a predefined way.

IV.5.4.6. Nanomanipulator:

The last method relies on the use of a tool which enables us to manipulate nanowire (Zyvex corporation). Since it is not really suitable to industry but rather for university research, I will not emphasize this part.

So, we have covered different ways to align nanowires. Some are not really efficient like using the laminar flow; other could damage the substrate such as using an electric field. Other seems to be promising like the Langmuir-Blodgett tool. Eventually, we could develop our own method to deposit Silicon nanowires on a patterned substrate. Even if this method seems not to be reliable, it could help us to deposit the nanowires on a desired location.

All these methods are linked to specific deposition process, that is to say the nanowires are removed from their substrates and deposited on other substrate.

IV.5.5. Process:

From now on, we assume that nanowires are well located and we can define the following process flow. This assumption is justified for deposition process in which nanowires are aligned. For a random growth, the process should the following way:

First we have to pattern on the substrate two crosses bar using photolithography that serve as the alignment marks. Then we grow the nanowires on substrate. We then locate a single isolated nanowire relative to the photographically defined alignment marks using optical microscope, SEM (scanning electron microscope), AFM (atomic force microscope). A layer of PMMA is then spin coated on top of the wires. PMMA is chemically sensitive to electron radiation, and will serve to define the electrode pattern. Before exposing the electrode pattern with electron beam radiation, however, we first align our coordinate system to the alignment marks on the substrate by using the electron

beam as a SEM. Care is taken not to expose the resist in the area near nanowire, as the SEM electron beam will also expose the PMMA resist. This is avoided by first finding alignment marks in the area away from the selected nanowire. We then turn off the electron beam and move the sample by the relative distance between the alignment marks and the selected nanowire, which has been recorded in the optical microscopy step, so that the electron beam will be centered on top of the wire. A computer file containing the desired electrode pattern is then loaded into the e-beam, and traces out the desired electrode pattern, writing the pattern into the PMMA. After the electron beam exposure, the PMMA is developed using a solution of 2:1 isopropanol:MIBK (methyl-iso-butylketone), which dissolves the exposed PMMA while leaving the unexposed PMMA in place. We then evaporate the metal for the contacts. Finally, the remaining unexposed PMMA is removed using NMP (1-methyl-2-pyrrolidinone) at 90 degree Celsius. At this point, all that is left on the substrate is the evaporated metal in those regions which had been exposed to the electron beam and the desired Si-nanowire underneath the electrodes.

In the previous parts, we have covered the process deposition, the catalyst deposition, the nanowire growth. Now, we will describe the process which is similar to the process used for a conventional MOSFET. Then, we will cover different issues such as doping, contact, improving performance, high K deposition, top gate.

The process used in this section relies only on one substrate that is to say we use the same substrate where nanowires were grown. Indeed, I don’t support this method since the growth of nanowires is random. The catalyst islands are well defined but we don’t control the direction of their growth. Consequently, we cannot assure that a nanowire will cross

the gap between the two islands over which metal will be defined. Let's describe the process:

First, the surface with thermally grown layer is cleaned with acetone, ethanol which silanized the surface as explained previously. Then, patterned catalyst Islands are defined with e-beam lithography. The process to deposit catalyst has been described in the previous part. So, we get patterned catalyst island. The substrate undergoes the growth process involving the VLS method described previously.

We then patterned a mask to define the source and drain, and the metal pattern is performed by evaporation generally TI/Au. Then we focus on the deposition of the high k material. For example, let' us consider the HfO2. HfO2 is deposited on the device at 300C using alternating surface saturating reactions of HfCl4 and H2O. (Stanford group) In that case, to get a conformal layer interface over the source and drain, we may use W. Then concerning the top gate, Electron-Beam lithography, metal evaporation (Ti/Au, 60 nm thick) and liftoff with slight overlap with the S and D are used to deposit the top gate.(Stanford group).

The process has been briefly overviewed in the previous part. We can now highlight some steps that can be useful to improve the performance of the nanowires-FET. Indeed, there will be some defects at the interface between the pure Si core and the SiO2 shell, these interface traps will modify the characteristic of the transistor. Consequently, this oxide coating may prevent good electrical contacts between S/D and Channel. In order to make reliable contact, it must be improved by reducing the thickness of the oxide coating or at least by passivating the interface traps. This may be achieved by different methods that we will review below:

IV.5.5.1. Reduction of the oxide shell:

Chemical etching of the oxide layer [34]:

Dai's group applied to the surface nanowires an HCl etching solution to remove the oxide layer on the nanowires. Then, Nws emanating from the patterned growth sites were contacted by metal source and drain.

Oxide reduction in a Hydrogen environment. [56]:

Yan'group reported that nanowires fabricated in a mixture of H2 and N2 prevent the formation of oxide coating. Still, this process has to be discussed since the diameter obtained with this mixture is much higher. To better understand this mechanism, let's us consider the following chemical reaction:

SiOx(s)+xH2->Si(s)+xH2O(g)

Through this equation, we can understand that the use of H2 may etch and may help to decrease the thickness of the SiO2 shell. Nevertheless, the presence of such a SiO2 layer may be helpful for the contact issue between nanowires and the metal (tunneling current).

IV.5.5.2. Passivation:

Thermal annealing. [32]:

Lieber's group performed a rapid thermal annealing in the forming gas to improve the contact and passivate Si-SiOx interface traps. Indeed a rapid thermal annealing was performed at 300-600C for 3min in the forming gas to passivate Si-SiOx interface traps.

A chemical passivation has been performed as well. Surface modification has been performed by reaction with 4-nitrophenyloctadecanoate. This specific molecule will lead to a stable and relatively nonpolar S-O-C.

IV.6. Summary of this chapter:

In this chapter, we have covered the different steps to build a nanowires-FET, we have unveiled and explained some interesting phenomena which appear during the process. Still, during the process, some issues will be raised and the characteristics of nanowires may be different from those predicted by the classical physics. These are the topics I will discuss about in the next chapter.

V. Issues to overcome:

After this process, we can predict some drawbacks. Consequently, we will discuss about the Gold tip, the problem related to the characterization and the doping phenomenon which represent a non-exhaustive list of inherent drawbacks. Then, we will apply the classical physics to nanowires to understand the effect of defects on their electrical properties.

V.1. Physical issues:

V.1.1. Gold tip:

As we have noted, the growth of the nanowires is improved by a catalyst. In that case, we use gold colloid. The problem with this catalyst is that gold tip:

- May cause a contamination of the nanowires
- May act as a dopant

Indeed, at 800C, Au metal will diffuse into the NWs. Au is a p-type dopant in Si. While Au can increase the carrier density for p-type NW, it may also decrease the carrier mobility because it acts as a scattering center [59].

Moreover Au lies close to the middle of the band gap; with such deep dopants levels in Silicon, only small amount of Au dopants atoms is expected to be ionized. It is known that the carrier concentration in the bulk Silicon with Au as its dopant will peak near $\sim 10^{12}$ carriers/cm^3, even though the number of Au atoms is significantly higher.

V.1.2. Resistivity:

Another drawback is the resistivity, it may differ from the bulk material and may help us to determine the mobility of carriers inside the nanowires. Let's consider the electrical resistance R of silicon nanowires which is given by:

$$R = \frac{\rho_{Si} L}{\pi r^2} \quad \textbf{(V-1)}$$

Where r is the radius of the silicon nanowires, L is the length and ρ_{Si} the resistivity of Silicon which is equal to $10\,\Omega.cm$.

We can deduce from the above equation the resistivity of the nanowires. The expected results can be a resistivity less important than in the bulk material which is due to the high carriers' mobility inside the nanowires.

To better understand this, let us consider the equation of the resistivity:

$$\rho_{Si} = \frac{1}{q(n\mu_n + p\mu_p)} \quad \textbf{(V-2)}$$

Taking care that some groups are evaluating the resistance of the nanowires rather than the contact resistance, we could determine the resistivity and deduce the mobility.

For instance, the resistivity obtained by UCLA groups is about $45\ \mathrm{m}\Omega.cm$ which is three orders less than at in silicon, which may be explained by an enhanced mobility.

V.1.3. Interface defects:

Another problem may be the interface defects. Indeed, the size of the nanowires does not allow to neglect the surface compared to the volume. It is well known that the interface between the silicon and the oxide has some defects. The presence on the surface of a native oxide is unavoidable. The density of these defects depends on the way of the oxide

has been grown. The order is about $10^{11}/10^{13}\,cm^{-2}$. To be aware of these orders, let's us consider a silicon nanowires of length $1\,\mu m$ and radius 10 nm. Let's consider a defect density of about $10^{12}\,cm^{-2}$. A simple calculus will gave for this nanowire a number of interface defects 400. Besides, if we consider a doping concentration of $10^{15}\,cm^{-3}$ which correspond to a presence of 0.1 carriers in the nanowires brought by the doping. There are two conclusions we can infer from this. On the one hand, the interface defect will play an important role and may deplete completely the nanowire inhibiting any circulation. On the other hand, it appears that the level of doping required to compensate the defects interface must be high: doping action should bring a number of carriers equal or more than to the number of defects to get free carriers in the nanowires. In this case, the doping concentration should be equal to $10^{19}\,cm^{-3}$. Such a doping corresponds to a presence of a dopant every 2nm in the silicon nanowires. This situation may damage the electrical transport, since dopants will induce local fluctuation of electrical potential which may induce some Coulomb Blockade Phenomenon.

V.2. Characterization:

Major drawbacks we will have to overcome are the different ways to characterize nanowires. Structural and geometrical factors play an important role in determining the various attributes of nanowires, such as their electrical and optical properties. Therefore, various novel tools have been developed and employed to obtain this important structural information at the nanoscale. At the micron scale, optical techniques are extensively used for imaging structural features. Since the sizes of nanowires are usually comparable to or, in most cases, much smaller than the wavelength of visible light, traditional optical

microscopy techniques are usually limited in characterizing the morphology and surface features of nanowires.

Therefore, electron microscopy techniques play a more dominant role at the nanoscale. Since electrons interact more strongly than photons, electron microscopy is particularly sensitive relative to x-rays for the analysis of tiny samples.

In this section we review and give examples of how scanning electron microscopy, transmission electron microscope are used to characterize the structure of nanowires

V.2.1. Scanning Electron Microscopy:

SEM usually produces images down to length scales of >10nm and provides valuable information regarding the structural arrangement, spatial distribution, wire density, and geometrical features of the nanowires.

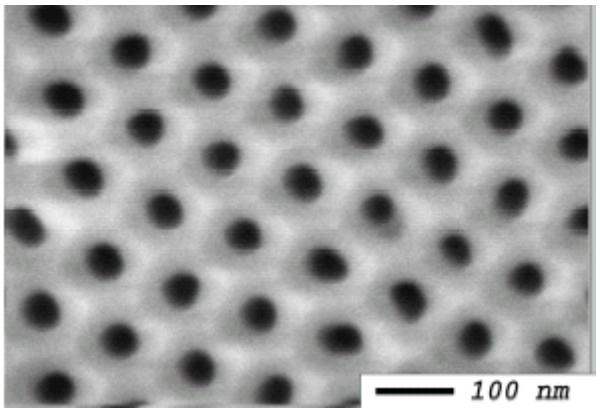


Figure V-1: SEM images of the top surfaces of porous anodic alumina templates anodized with an average pore diameter of 44nm [73]

Example of SEM micrographs shown in Figs.V.1 indicates that structural features at the 10nm length scales can be probed, providing information on the size, size distribution, shapes, spatial distributions, density, nanowire alignment, filling factors, etc. As another example, Fig.V.2(a) shows an SEM image of ZnO nanowire arrays grown on a sapphire

substrate [60], which provides evidence for the non-uniform spatial distribution of the nanowires on the substrate, which was attained by patterning the catalyst film to define high density growth regions and nanowire-free regions. Figure V.2(b), showing a higher magnification of the same system, indicates that these ZnO nanowires grow perpendicular to the substrate, and are well-aligned with approximately equal wire lengths and have wire diameters in the range from $20 < d < 150$ nm.

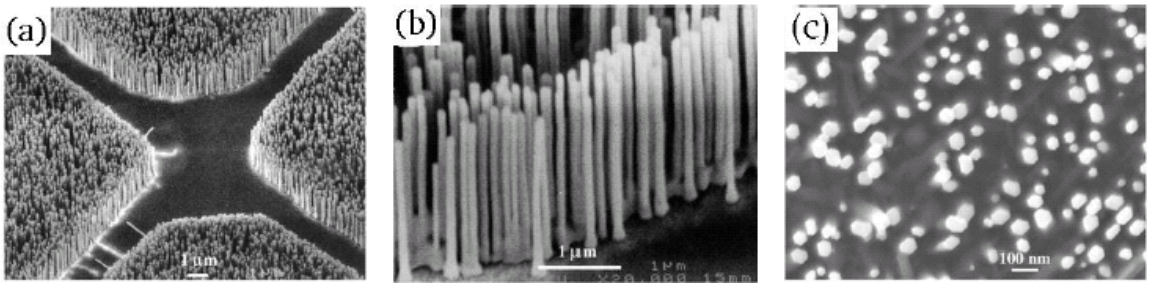


Figure V-2: SEM images of ZnO nanowire arrays grown on a sapphire substrate [60].

Figure V.3 shows an SEM image of GaN nanowires synthesized by a laser-assisted catalytic growth method [61], indicating a random spatial orientation of the nanowire axes and a wide diameter distribution for these nanowires, in contrast to the ZnO wires in Fig. V.2.

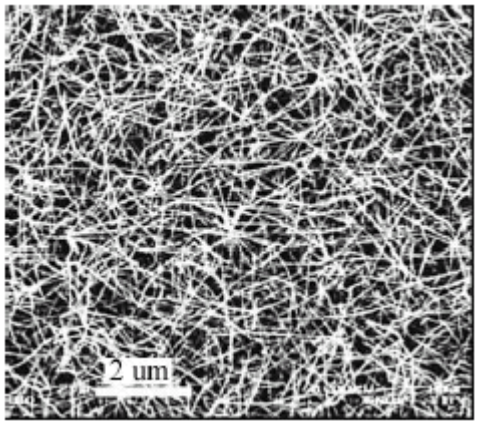


Figure V-3: SEM image of GaN nanowires in a mat arrangement synthesized by laser-assisted catalytic growth. [61]

V.2.2. Transmission Electron Microscopy

TEM and high resolution transmission electron microscopy (HRTEM) are powerful imaging tools to study nanowires at the atomic scale, and they usually provide more detailed geometrical features than in SEM images. TEM studies also give information regarding the crystal structure, crystal quality, grain size, and crystal orientation of the nanowire axis.

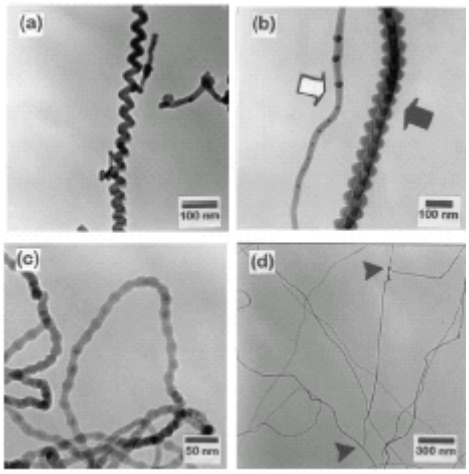


Figure V-4: TEM morphologies of four special forms of Si nanowires synthesized by the laser ablation of a Si powder target. [62]

When operating in the diffraction mode, selected area electron diffraction (SAED) patterns can be made to determine the crystal structure of nanowires. For example, the TEM images in Fig. V.4 show four different morphologies for Si nanowires prepared by the laser ablation of a Si target [62]: (a) spring-shaped; (b) fishbone-shaped (indicated by solid arrow) and frog-egg-shaped (indicated by the hollow arrow), (c) pearl-shaped, while (d) shows the poly-sites of nanowire nucleation. The crystal quality of nanowires is revealed from high resolution TEM images with atomic resolution, along with selected

area electron diffraction (SAED) patterns. For example, figure V.5 shows a TEM image of one of the GaN nanowires, indicating single crystallinity and showing (100) lattice planes, thus indicating the growth direction of the nanowire, and this information is supplemented by the corresponding electron diffraction pattern in the upper right.

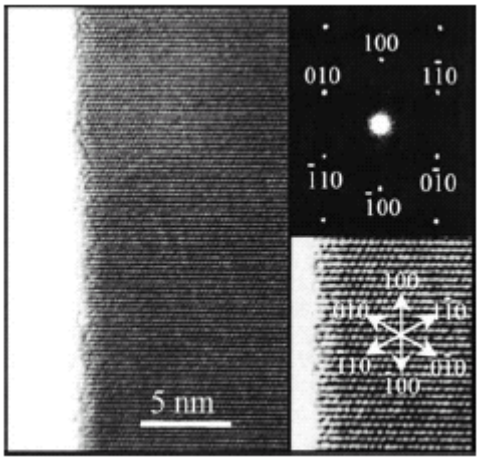


Figure V-5: Lattice resolved high resolution TEM image of one GaN nanowire (left) showing that (100) lattice planes are visible perpendicular to the wire axis. A lattice-resolved TEM image (lower right) highlights the continuity of the lattice up to the nanowire edge, where a thin native oxide layer is found. The directions of various crystallographic planes are indicated in the lower right figure [61].

The high resolution of the TEM allows also for the investigation of the surface structure of the nanowires. In many cases the nanowires are sheathed with a native oxide layer, or an amorphous oxide layer that forms during the growth process. This can be seen in figure V.6 for germanium nanowires [63], showing a mass-thickness contrast TEM image and a selected-area electron diffraction pattern of a Ge nanowire. The main TEM image shows that these Ge nanowires possess an amorphous GeO2 sheath with a crystalline Ge core that is oriented in the [211] direction. Dynamical processes of the surface layer of nanowires can be studied by using an in situ environmental TEM chamber, which allows TEM observations to be made while different gases are introduced or as the sample is heat treated at various temperatures.

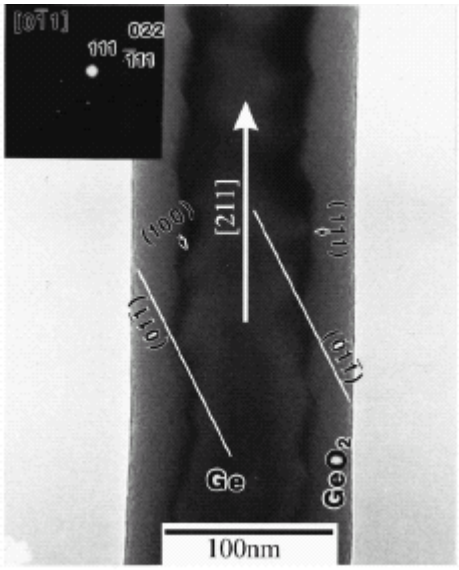


Figure V-6: A mass-thickness contrast TEM image of a Ge nanowire [63].

V.3. Modeling and Simulation:

Another question which could be raised is: Do the electrical characteristics of silicon nanowires follow the scale law? Previously, we have reported the nanowires don't work like a conventional MOSFET. The question raised now, is a nanowire a thin wire? Besides, we reach some scale where surfaces can not be neglected compared to the volume (L^2 / L^3 increases), which can turn the nanowires into insulator because of the depletion of carriers on the surface. Does the law which binds the dimensions to the resistivity still valid? What is the role of the doping when the distance between dopants are the same order than the dimension of the circuit?

To be able to answer to these questions, we should model the scheme at room temperature based on the classical physics.

V.3.1. Contact:

In an experiment to study electrically nanowires, the length of the electrode and consequently the resistance depends on the layout of the electrode. In case where electrodes are long, the value of the resistance will be several orders of magnitude higher than the one expected from the nanowire at room temperature. Consequently, it could be neglected in the following part. We have also to deal with the interface between the metal and the nanowires. For this, we have to refer to the Schottky diode and the related energy band diagram. Indeed, every semiconductor is inevitably linked to a metal. It is necessary that the contact between metal and semiconductor shows a resistance as low as possible. For this, we decrease the resistance by heavily doping the part of the conductor where the contact is realized. With a high doping ($>10^{19} cm^{-3}$), the thickness of the depletion region is so low that carriers can cross the barrier by tunneling. The device shows an characteristic symmetrical I(V), a low resistance and can act as an Ohmic contact.

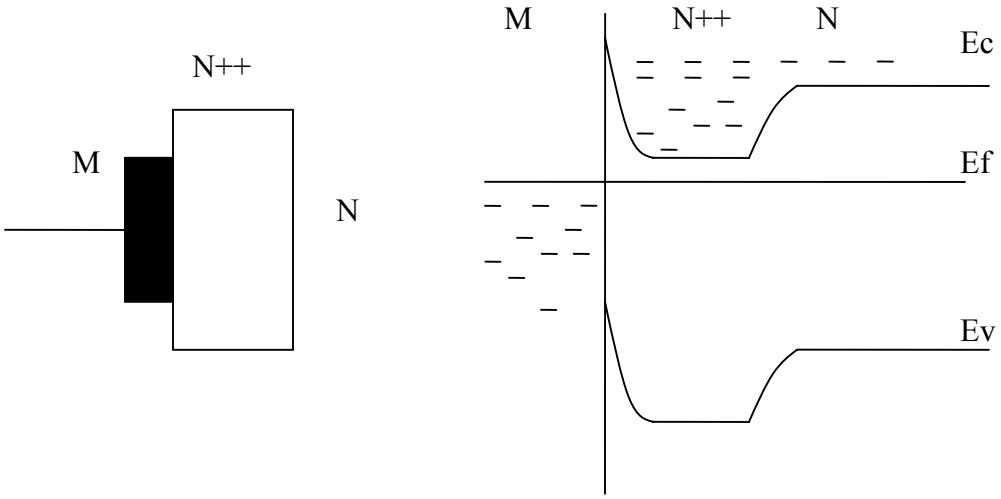


Figure V-7: Metal Nanowire contact and Energy band diagram

For the N++/N transition, accumulation of electrons comes up in the interface side N. There is no region with majority carriers. Only the resistance of the semiconductor induces the drop of tension in the structure as shown on figure V-7. At the contact, the incoming or exiting electrons in the N region is compensated by the incoming or exiting electrons in the N+. The current flows freely in the two ways.

V.3.2. Nanowires:

The modeling of the nanowire structure can quickly become complex. Thus, we will begin with the approximation of an isolated wire, without interface state and having the same mobility as the substrate with the same doping. The scheme of the wire is draw below. We define the radius by r and the length by L.

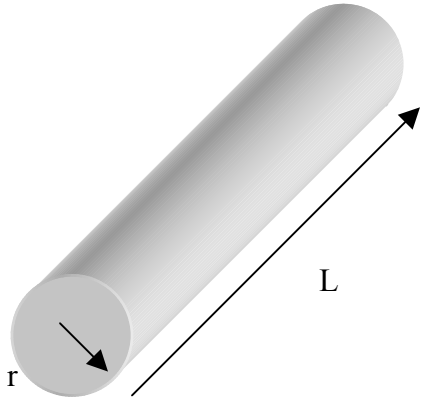


Figure V-8: Scheme of a nanowire.

The current of Drain-Source is given by:

$Ids = j_{ds} 2\pi r^2 = N_d e \mu_n 2\pi r^2$ **(V-3)**,

with j_{ds} the density of the current in the nanowire, e is the absolute value of the electron charge and μ_n the mobility of carriers. The mobility depends principally on the doping, the temperature, the electric field and the quality of the materials. The temperature is fixed at room temperature, that is to say 300K. The mobility curve $\mu(Nimp)$ for n and p materials type is represented in the following picture (figure V.9) in the case of substrate silicon with doping Nimp. μ_n and μ_p are the mobility of silicon of n and p type respectively.

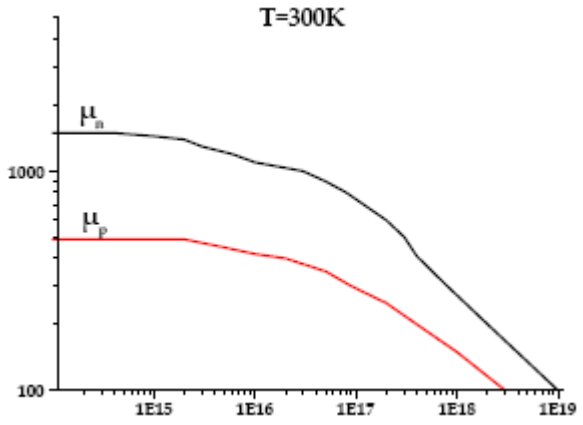


Figure V-9: Mobility with the density of states at T=300K for a silicon substrate [40]. On x axes, it is shown concentration and on y axes, the mobility.

This expression doesn't take into account the electric field. This high field is given by:

$$\mu = \frac{\mu(Nimp)}{1 + \frac{\mu(Nimp) * |E_x|}{vsat}} \quad \text{(V-4)}$$

and the drift velocity $vd = \mu * E_x$ with vsat the saturation velocity. Figures V.10 and V.11 represent the effect of electric field for three doping concentrations.

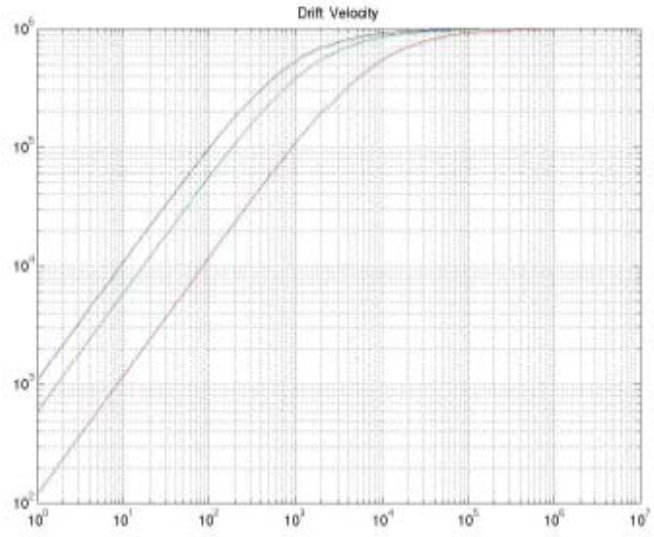


Figure V-10: Drift velocity ($cm.s^{-1}$). Doping are $Nd = 10^{16}\,cm^{-3}$ (upper curve), $Nd = 2.10^{17}\,cm^{-3}$ (middle curve) and $Nd = 10^{19}\,cm^{-3}$ (lower curve).

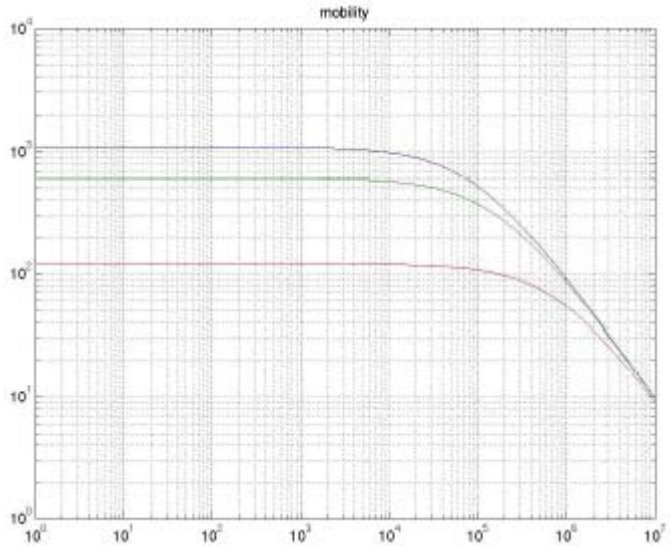


Figure V-11: mobility ($cm^2.V^{-1}.s^{-1}$) related to electric field. Doping are $Nd = 10^{16}\,cm^{-3}$ (upper curve), $Nd = 2.10^{17}\,cm^{-3}$ (middle curve) and $Nd = 10^{19}\,cm^{-3}$ (lower curve).

The current density j_{ds} depends on the drift velocity through the expression $j_{ds} = e * N_d * vd(E_x, Nimp)$ (V-5). We approximate Ex with Vds/L which

represents the average electric field on the length of the nanowire. Figure V.12 shows the current density for the same doping concentration as figure V.11.

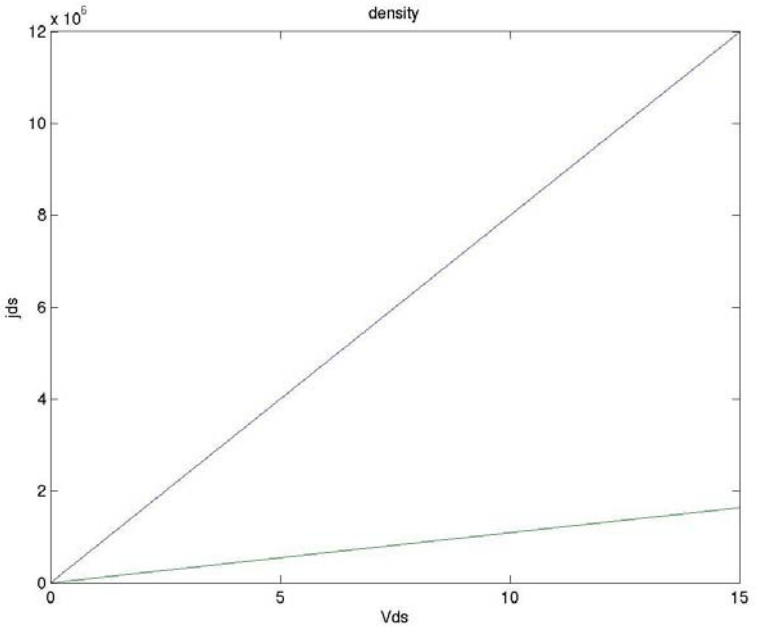


Figure V-12: Density of current ($A.cm^{-2}$) versus Vds ($Nd = 2.10^{17}\,cm^{-3}$ lower, $Nd = 10^{19}\,cm^{-3}$ upper).

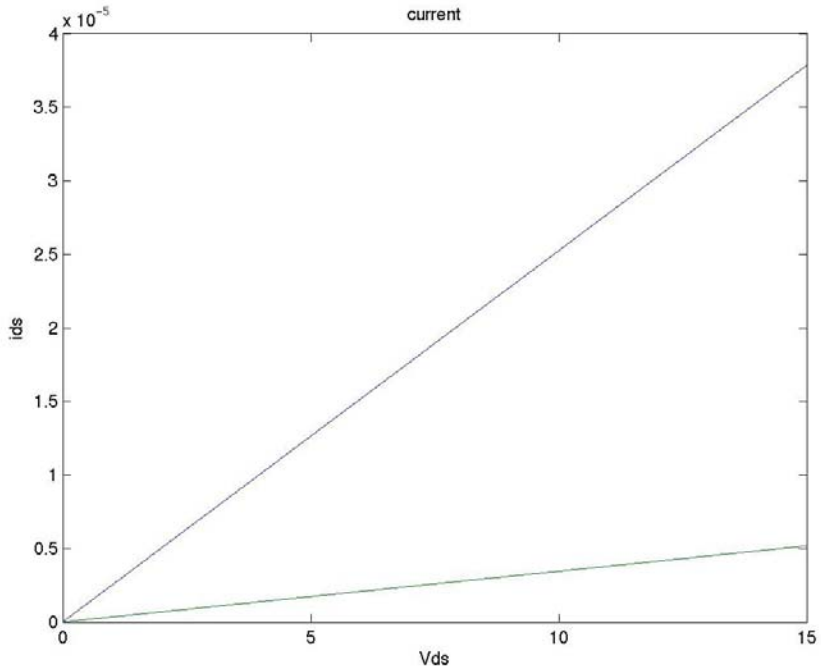


Figure V-13: current (A) versus Vds (V) ($Nd = 2.10^{17}\,cm^{-3}$ **lower,** $Nd = 10^{19}\,cm^{-3}$ **upper).**

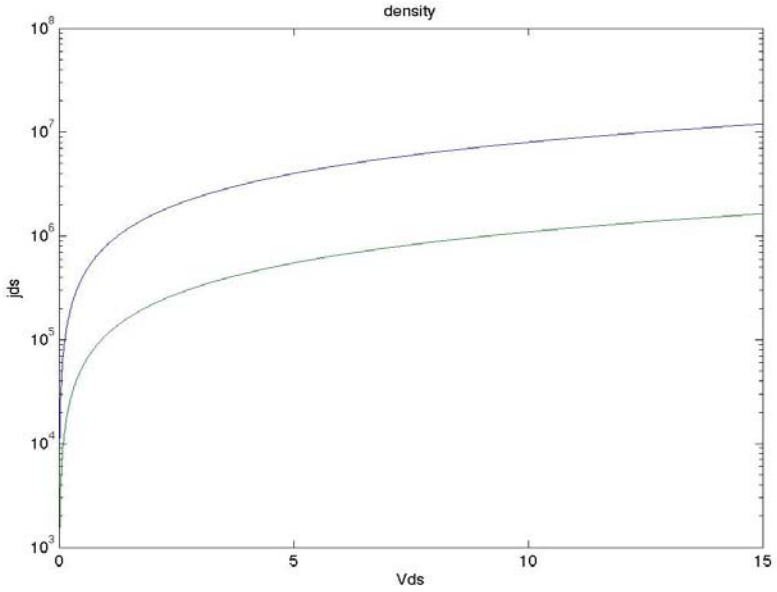


Figure V-14: Log Density of current ($A.cm^{-2}$ **) versus Vds (V) (** $Nd = 2.10^{17}\,cm^{-3}$ **lower,** $Nd = 10^{19}\,cm^{-3}$ **upper).**

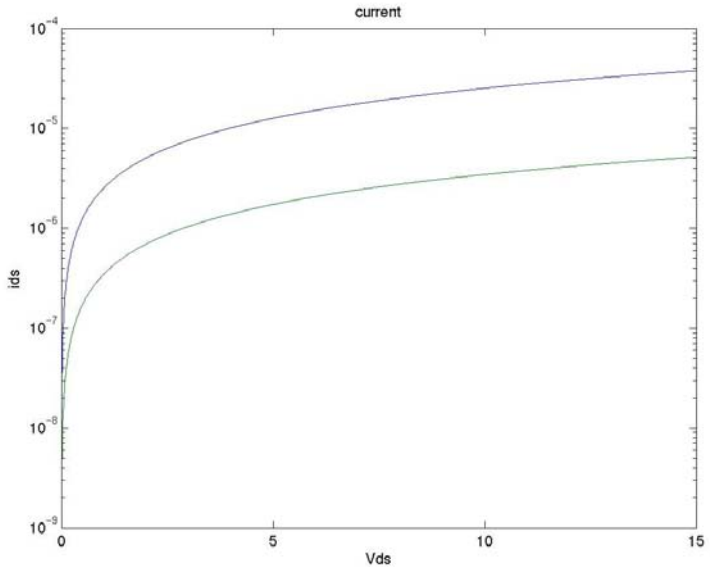


Figure V-15: Log current (A) versus Vds ($Nd = 2.10^{17}\,cm^{-3}$ **lower,** $Nd = 10^{19}\,cm^{-3}$ **upper).**

The current saturation should be differentiated from the electric field in the transistor. Both could be correlated as we will see in the following. From the previous simulation, we can deduce that the resistances are respectively 315kOhm and 41kOhm for $Nd = 2.10^{17} cm^{-3}$ and $Nd = 10^{19} cm^{-3}$. We can deduce the effect of the radius and the length on the current drain-source for a nanowire doped at $Nd = 10^{19} cm^{-3}$ as shown in figures V.16 and V.17.

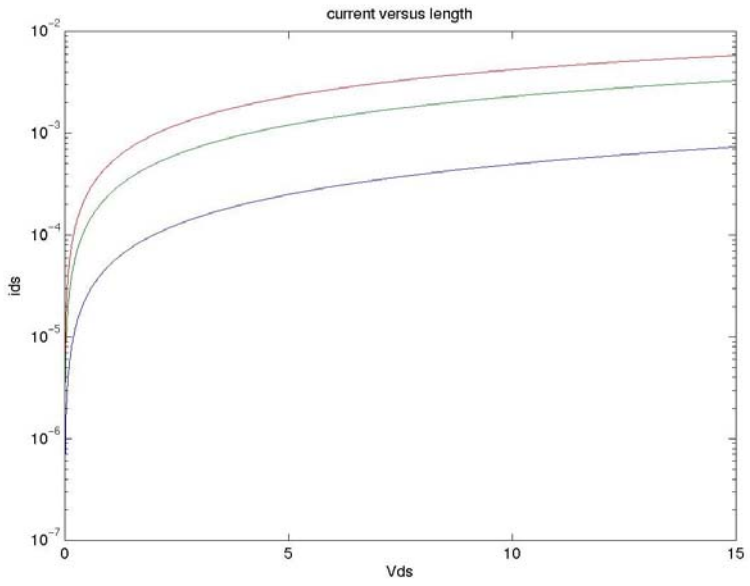


Figure V-16: Ids(A)-Vds(V) for radius r=10nm and $Nd = 10^{19} cm^{-3}$. Length are from the upper are L=500nm, L=1um and L=5um.

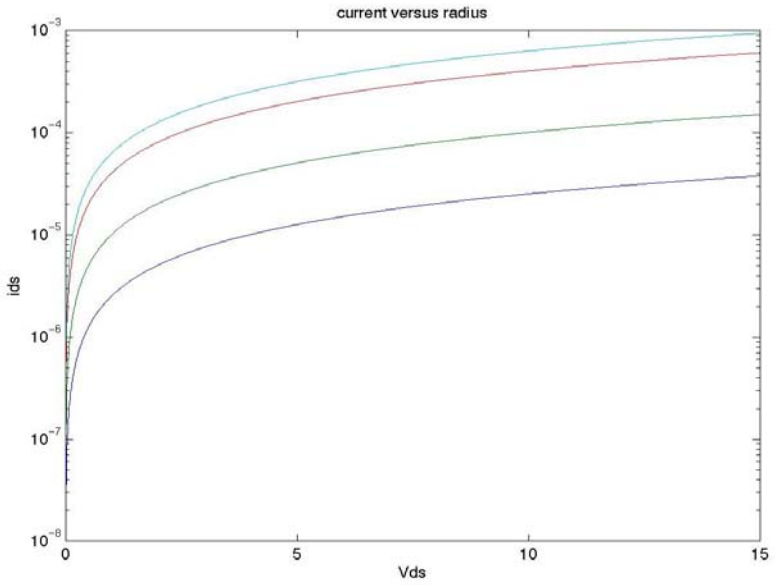


Figure V-17: Ids(A)-Vds(V) for L=1um and with $Nd = 10^{19} cm^{-3}$. The radius are from the bottom, 10, 20, 40, 50 nm.

From the equation, we can deduce that the length affects directly the saturation because of E=Vds/L whereas the surface will affect the slope at the origin.

V.3.3. Interface states:

The previous approach is suitable for high dimensions where the interface states can be neglected. Still, this simulation represents an ideal case for nanowires. Indeed, the interface states will build a depletion region which can turn the nanowire into insulator depending on the doping. To better understand the effect of the interface states in the nanowires at room temperature, we will propose a simple model with depletion region in zone I and a conductor region II (figure V.18).

First, we will consider the width of the depletion region as a constant for all the interfaces, and then we will do a more detailed simulation in function of the density of states and the doping. Then, we will deduce the variation of potential to the associated surface.

For weak bias Vds and by considering Seff, the effective section, the resistance

$$R = \rho.L / Seff = \frac{R_o}{\left(1 - \frac{d}{r}\right)^2}$$

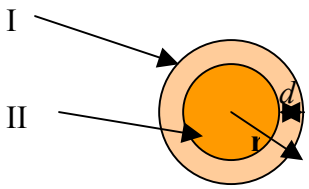


Figure V-18: Cross section of a nanowire with the depletion region

Take into account L and r which are variable, figure V.19 represents the variation of the normalized resistance to Ro (value of the resistance without depletion region) with radius for different values of depletion d.

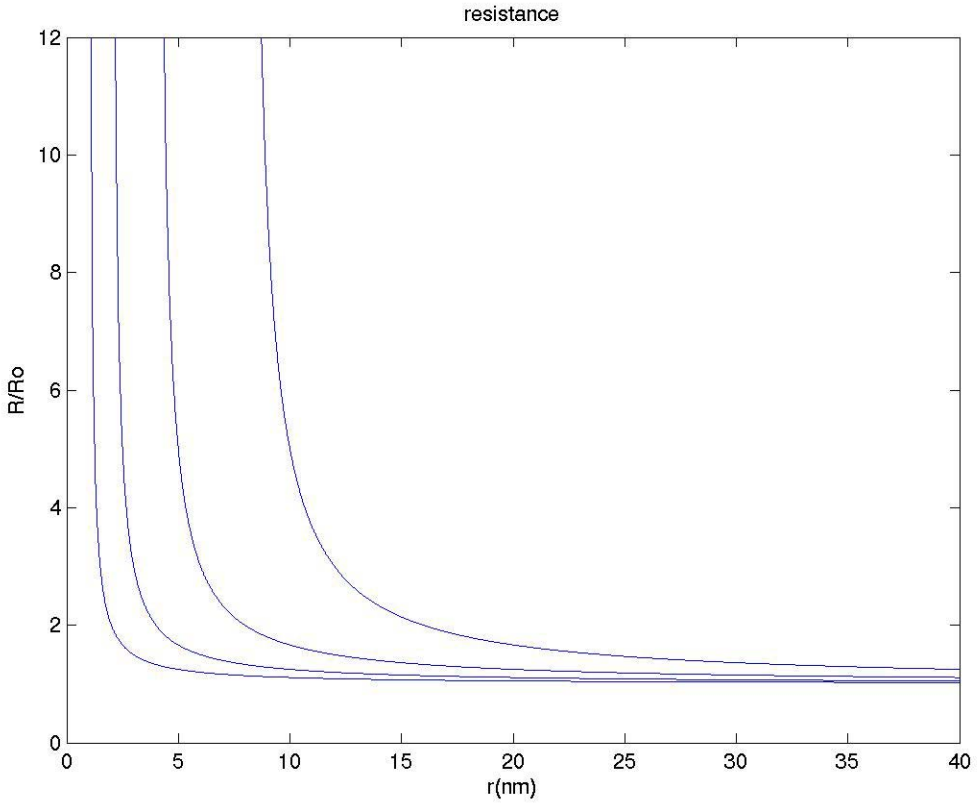


Figure V-19: evolution of the resistance (normalized to resistance for d=0) with the radius for different values of d (d=1, 2, 3, 4, 8 from the bottom).

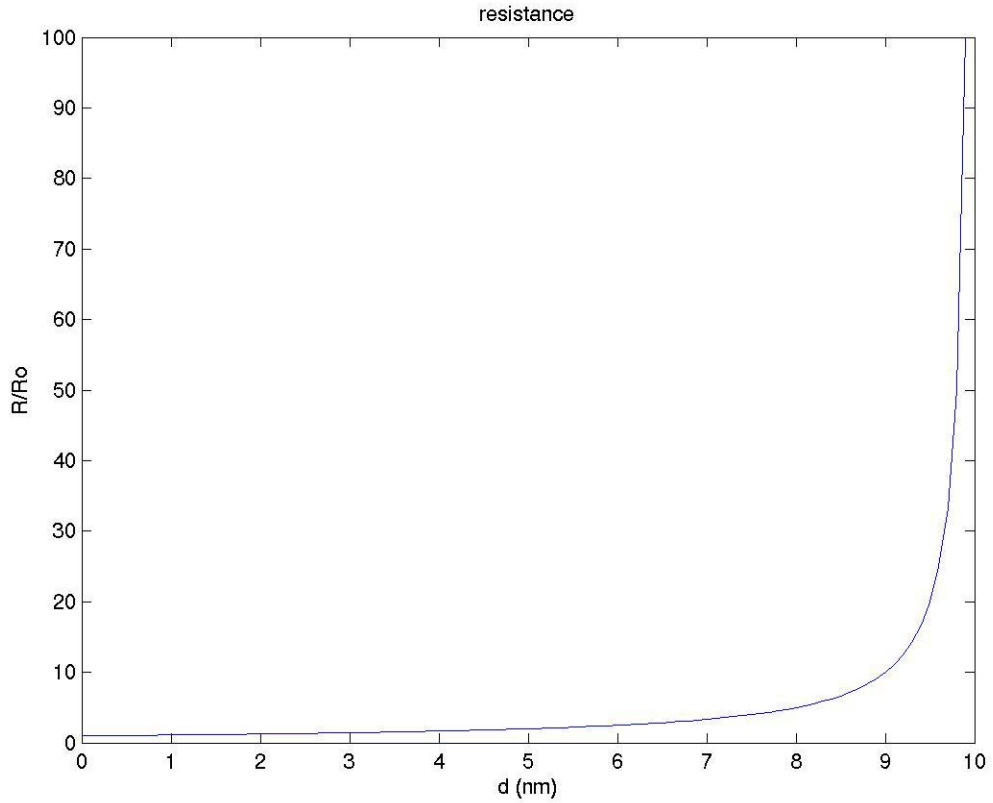


Figure V-20: evolution of the resistance (normalized to resistance with d=0) with the thickness of the depletion for a radius r=10nm.

The simulation in figure V.19 and V.20 show principally two effects: first, the resistance is higher than Ro for nanowires. It reaches 2Ro for d=3nm and 5Ro for d=8nm and it is infinite for d=10nm taking into account a radius r equal to 10nm. Then, scale law is not valid for radius less than 40nm.

We are going to express d in terms of the doping and the density of interface states to have an idea of the wire depletion. Ec is the value of the conduction band, Ev is the value of the valence band and Ef Fermi level. There is a charge transfer from silicon to the

interfaces states located to the level Et because (Ec-Et)>(Ec-Ef) and, thus, surface level has to be fulfilled in fig V.20. There is a space charge region consequently:

$$e\Phi s = Ec(0) - Ec(\infty) > 0 \quad \textbf{(V-6)}$$

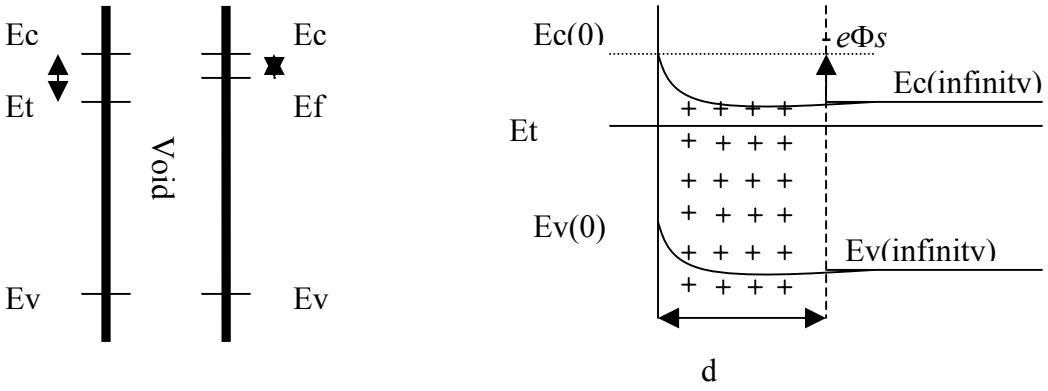


Figure V-21: Energy band diagram of silicon interface.

The repartition of the interface states in the Silicon forbidden band gap has already been studied [64], [65], [66], [67]. The picture in fig V.21 represents the main state groups according the Flietner model [68], they are results from defects due to pending bond according different configurations. The U distribution of the interface state can be seen as the superposition of two contributions:

States Ut near the conduction band are due to constraint bonds ($Si_3 \equiv Si - Si \equiv Si_3$) and states Um located symmetrically around the minimum near the middle of the forbidden band gap resulting form the pending bond ($Si_3 \equiv Si -$). Moreover, the groups in Gaussian distribution can be seen in the upper and lower middle part of the forbidden band gap Pl and Ph respectively.

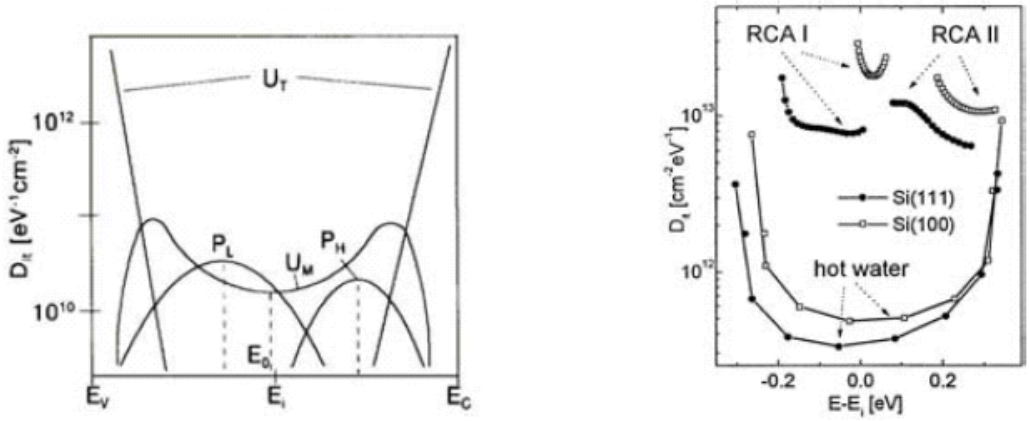


Figure V-22: states repartition at the Si/SiO2 interface [64], distribution of interface states Dit(E) for Si(111) and Si(100) after RCA and Hot Water [65]

The experiments are in agreement with this distribution. The density of states depends on the preparation of surface. For instance a surface passivated with Hydrogen gives a low interface state density, but an encapsulation in DI water (80C, 90min) gives excellent results as well compared to classical method and decreases the roughness [69].

First, we consider interfaces states located at energy $\Delta_t = 0.3eV$ in the conduction band with a density $N_{ss} = 10^{12} cm^{-2}$. We can now build a model corresponding to the picture above.

The Fermi level in the volume is located at energy $\Delta F_\infty = E_{c(\infty)} - E_F = kT \ln(N_c / N_d)$ from the conduction band where k is Boltzmann constant, T temperature (K) and Nc is the equivalent density of states in the conduction band. $\Delta F_\infty = 0.12eV$ for $Nd = 2.10^{17} cm^{-3}$ and 0.03eV for $Nd = 10^{19} cm^{-3}$. In the last case, we are at the edge of using this expression.

In the Poisson equation, we get $d = \sqrt{\frac{2\varepsilon(-\Phi s)}{eNd}}$ which is a result with the surface potential Φs. ε is the dielectric permittivity of silicon (ε_0 dielectric of void multiplied by ε_r the relative permittivity of Silicon). Thus to know the depletion width, we have to express the surface potential. The charge of this region is defined by the following expression: $Q_{vol} = e.Nd.d = \sqrt{2e\varepsilon Nd(-\Phi_s)}$. We defined Qss (e*Nss) as the stocked charge on the surface acceptor states per area unit. The probability of occupation of these states follows the Fermi Statistic: $f(Et) = \frac{1}{1+\exp(\frac{E_T - E_F}{kT})}$ and

$$Qss = -eNss(f(Et)) = -eNss *$$

$$Qss = \frac{-eNss}{1+\exp(\frac{E_t - E_f}{kT})} = \frac{-eNss}{1+\exp(\frac{\Delta F_\infty - \Delta T}{kT})\exp(\frac{-e\Phi_s}{kT})} \quad \textbf{(V-7)}$$

With the electro-negativity, we get $Q_{vol} + Q_{ss} = 0$. We got the final equation:

$$f(Us) = 0 \text{ with } f(Us) = \frac{1}{1+a\exp(-Us)} - b\sqrt{-Us} \quad \textbf{(V-8)}$$

$$a = \exp(\frac{\Delta F_\infty - \Delta_T}{kT})$$

$$\text{where } b = \sqrt{\frac{2Nd\varepsilon kT}{e^2 Nss^2}} = \sqrt{2}Ld.\frac{Nd}{Nss}$$

$$Us = e\Phi s / kT$$

Where Ld is the Debye length which is related to the dielectric relaxation time by $Ld = \sqrt{D\tau_r} = \sqrt{\frac{\varepsilon kT}{e^2 Nd}}$. We can get the results by dichotomy by fixing the limit $-1 < \Phi_s < 0$, please refer to the Appendices A.1 for resolving this equation.

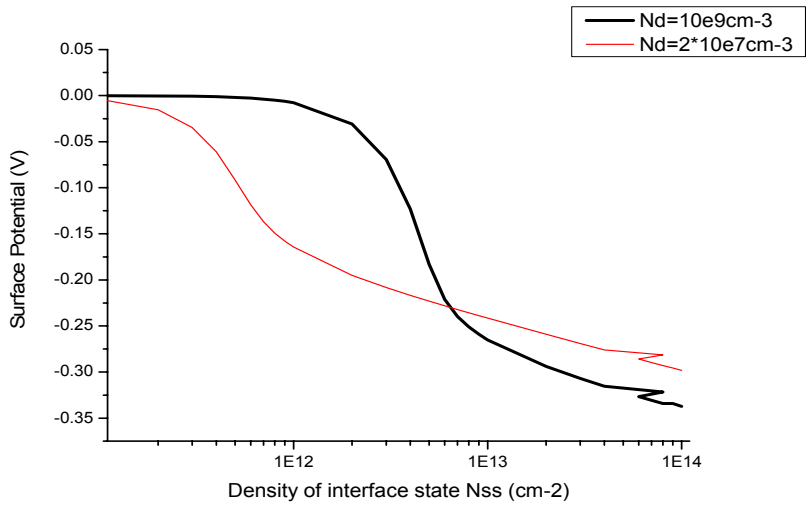


Figure V-23: Surface potential (V) with Density of interface states (cm^{-2}).

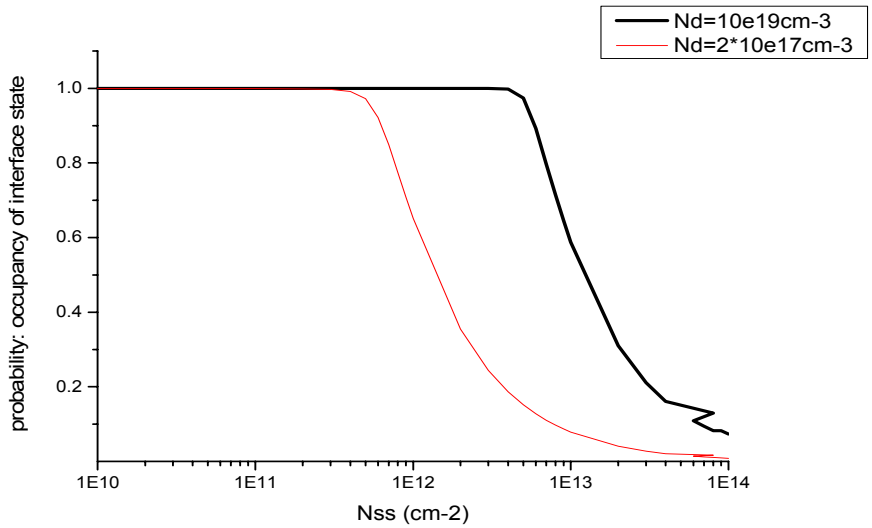


Figure V-24: Probability of interface states occupancy with the density of states (cm^{-2}).

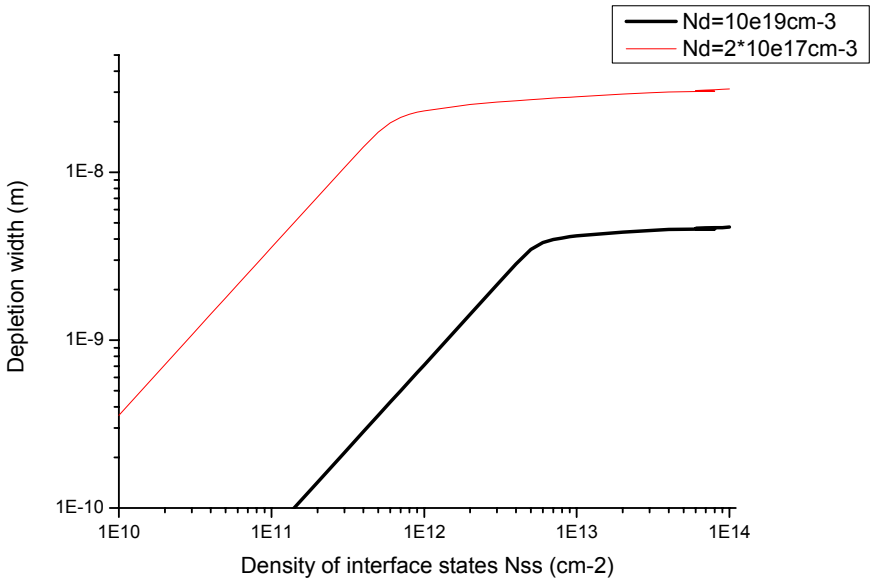


Figure V-25: Depletion width (m) with density of interfaces states.

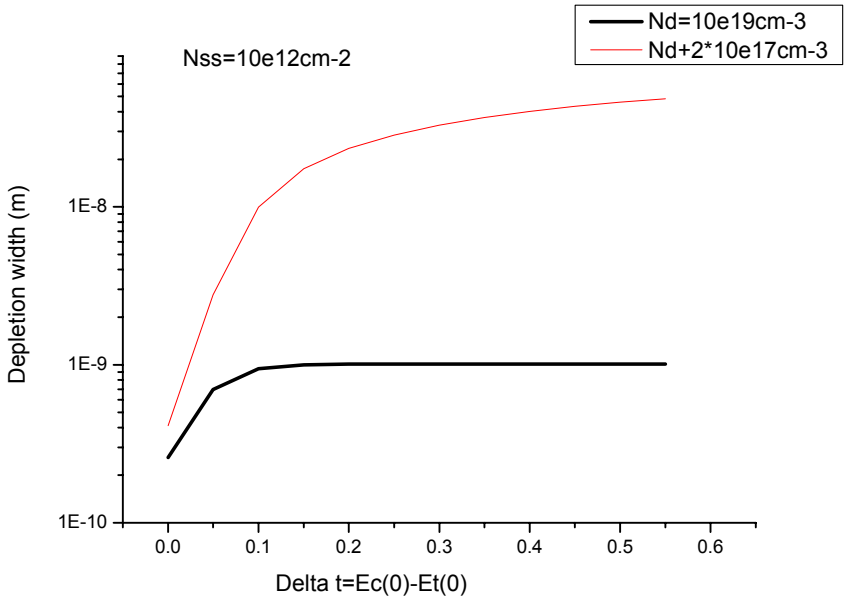


Figure V-26: Depletion width (m) with Δ_t

These simulations are very interesting to know the consequences of the interface states.

The figure V.25 shows the dependence of doping on the depletion width. This is much more spread in low doping ($2.10^{17} cm^{-3}$) and cause a total depletion of the nanowire for low density of interface states. The depletion in a nanowire with a doping $Nd = 10^{19} cm^{-3}$ is very sensitive to interface states for density comprised between $10^{11} cm^{-2}$ and $5.10^{12} cm^{-2}$. So, a good interface can turn off the depletion space. We can note that the depletion experiences a saturation.

The figure V.23 gives us the evolution of surface potential caused by the interface states for same doping as the figure V.25.

With the gate, this potential can be modulated till the space charge disappears.

According to the figure V.22, we have fixed $\Delta_T = 0.3eV$. We calculate the depletion width with Δ_T for previous chosen doping to know the consequences related to this unknown. The probability of filing is lower when Δ_T tends to 0, but the density of interface states is higher. Thus the chosen value seems to be in agreement with a maximal depletion for a doping $Nd = 10^{19} cm^{-3}$. The probability of interface states being occupied with changing density of interface states is represented in the figure V.24.

We have just seen that the spread of the space charge region caused by the interface states is the same order of magnitude of the radius of our nanowire. Thus, simulations on the evolution of the resistance according to the circuit scale and depletion width show their utility. We have seen that nanowires with a doping are naturally depleted at room temperature and consequently the use of gate is compulsory to do electrical measurement. In this simulation, we have neglected the charge effect of insulator. Indeed, there are

electric charges which may induce an electrostatic force on the carriers of the semiconductor [70] (SiO2 there are generally positive charge $10^{12}/10^{13} cm^{-3}$). The consequences are just a translation of the surface potential in the opposite direction of this induced by the interface states.

V.3.4. Diffusive reflection at interfaces:

It is known that the resistivity of thin film increases when the thickness is lower than the mean free path of electron. Fuchs [71] and Sondheimer [72] (FS theory) has allocated this effect to the diffusive reflection on the film edge. As the resistivity is inversely proportional to mean free path, it increases.

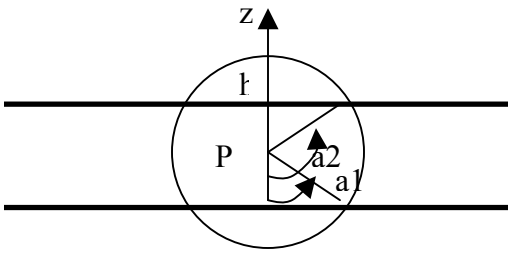


Figure V-27: Scheme of the mean free path in a nanowire.

We notice that the mean free path is only equal to the mean free in volume path for angles a1<a<a2. In other case, it depends on the angle a according to the following equation:

$\lambda(a) = z/\cos a$ for such as 0<a<a1 and $\lambda(a) = z - h/\cos a$ for a such as a2<a<π. By integrating the three regions, we get the following expression of the mean free path:

$$\frac{\lambda}{\lambda_o} = (3h/4\lambda_o) - (h/2\lambda_o)\ln(h/\lambda o) = \frac{\sigma}{\sigma_o} \quad \textbf{(V-9)}$$

where σ is the conductivity in the film and σ_o in the volume. The graph related to this equation is drawn below figure V.28:

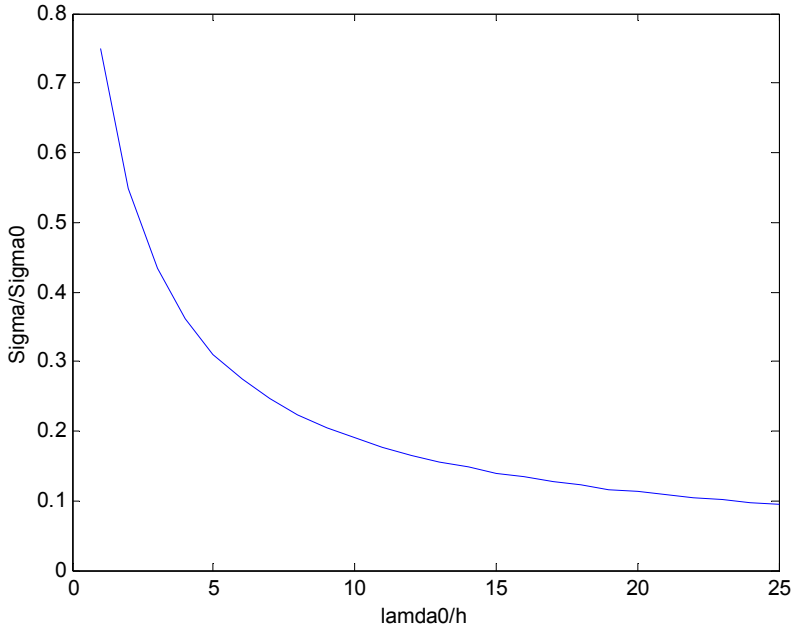


Figure V-28: diffusive reflection effect.

The consequence is a decrease of the mobility in thin film. In case of nanowire with a 10nm radius and a mean free path of 50nm, FS effect leads to a decrease of 50% of the conductivity.

V.3.5. Back gate effect:

V.3.5.1. Flatband voltage:

As we have seen in some reports, groups used back gate to control the device. Let's describe this effect to better understand the mechanism. Thus, we have seen in the previous parts that interface states and surface states could play a role on the band curve of semiconductor and drive to a complete depletion of our nanowire. In this case SIS

(Silicon Insulator Silicon), there is a supplementary modification due to a different workfunction (Figure V.29).

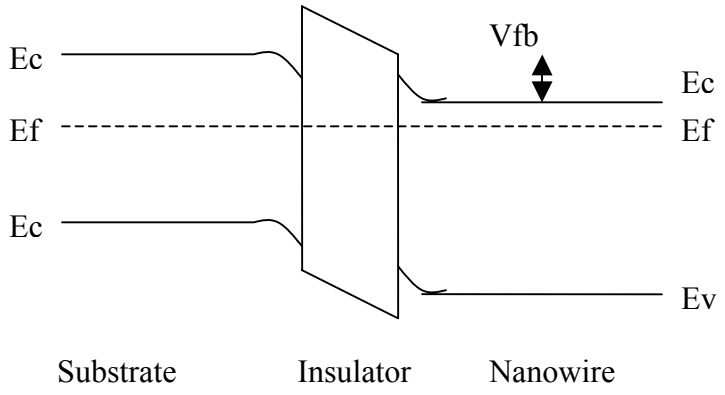


Figure V-29: Cross section of the SIS structure.

The bias to apply to get flat band is shown as Vfb in figure V.29.

Thus, taking into account the difference of the workfunctions and the presence of interface states, the bias required to get plate band is:

$$Vfb = \left[(\Phi_{sbulk} - \Phi_{sfilm}) - \frac{Q_{ss}}{C_{ox}} \right] \quad \textbf{(V-10)}$$

We consider that the substrate is P type with $Na = 5.10^{14}\,cm^{-3}$. So:

$e\Phi_{sbulk} - e\Phi_{sfilm} = kT \ln(Na * Nd / ni^2) = 0.69eV$ for $Nd = 2.10^{17}\,cm^{-3}$

=0.76eV for $Nd = 10^{19}\,cm^{-3}$

The number of occupied state is not equal to the number of interface states. We have to take into account the probability of occupancy P in the calculation of Vfb. For an energy level located at 0.3eV from Ec, we have the following relation between Nss* and Nss:

$eNss^* = -eNss.f(Et)$

Cox, oxide capacity is defined by $\varepsilon_0 \varepsilon_{ox} / d_{ox} = 8{,}8.10^{-9} F.cm^{-2}$ (dox, thickness of the buried oxide 400nm). So we get the following curve figure V-30. Vfb is shown in figure V-31.

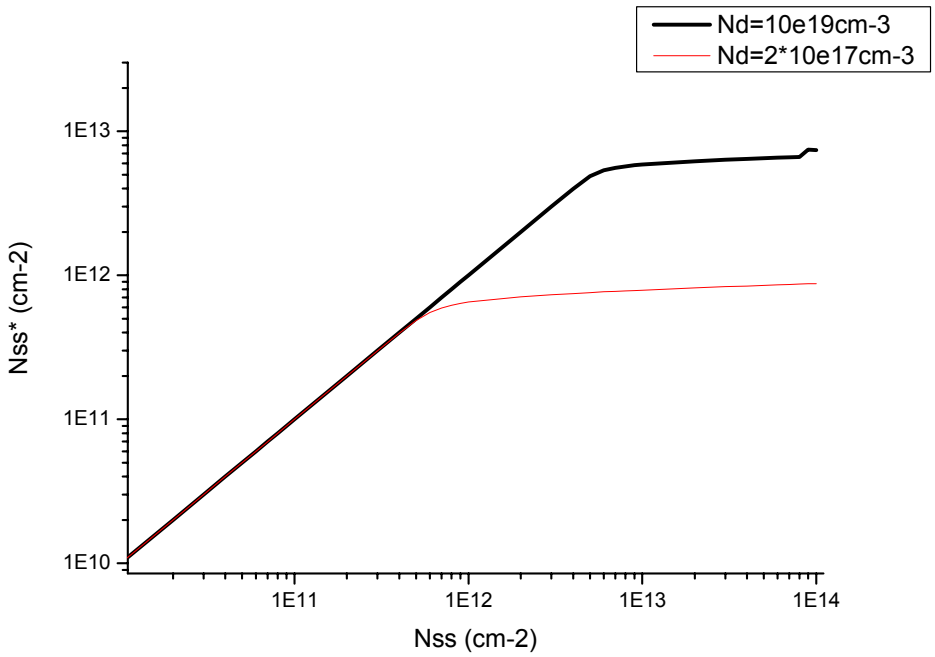


Figure V-30: occupied interface states with the density of interface states.

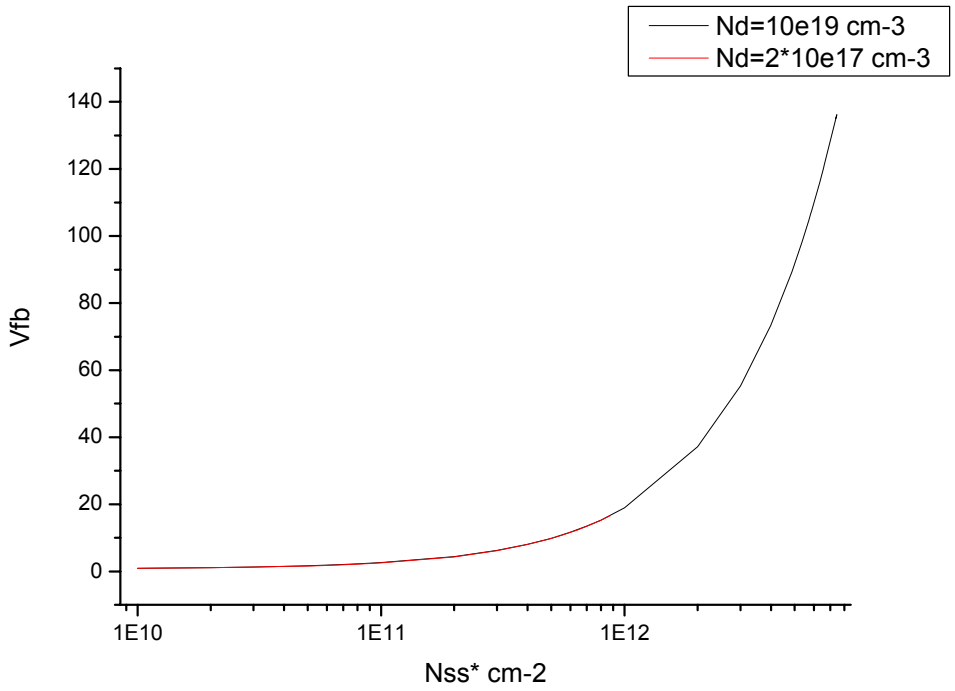


Figure V-31: Flatband voltage with the density of interface states Nss* (cm^{-2}) for different dopings $Nd = 2.10^{17} cm^{-3}$ and $Nd = 10^{19} cm^{-3}$.

V.3.5.2. SIS structure:

Vfb is high because of the thickness of the oxide. The effects of the workfunction difference and the presence of the interface states are added to the effect of the bias, thus we will determine the effect of the last by neglecting the first ones. We will have to add them to the final result. Trough the following figure V-33, we can notice the dependence in different regions: an exponential dependence in accumulation, an $V^{1/2}$ in depletion and exponential in strong inversion.

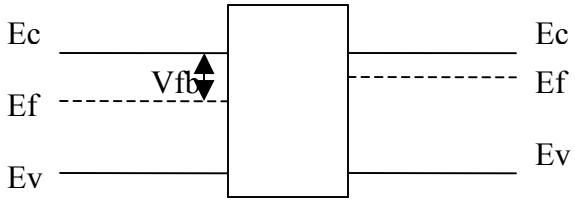


Figure V-32: Energy band diagram after application of Vfb.

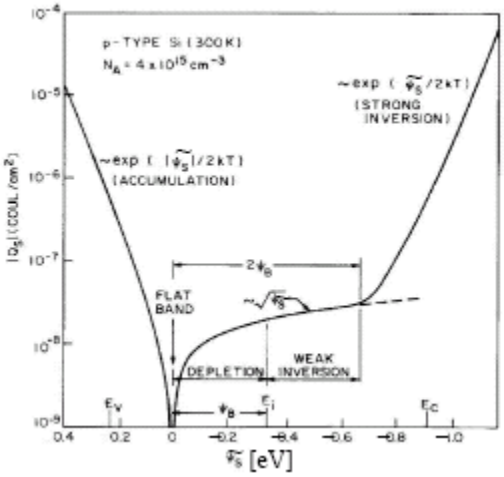


Figure V-33: Space charge space density in a p-type semiconductor with $Na = 4.10^{15} cm^{-3}$ **[72].**

In our case (n type), the surface potential is of opposite sign. So, for Vs>0, Qsc is negative, the structure is in accumulation.

$$Qsc \approx \frac{\varepsilon skT}{eLd}\sqrt{\frac{eVs}{kT}} \quad \textbf{(V-11)}$$

The space charge is negative and increases exponentially with the bias. If it is an accumulation charge, its spread is relatively low (Page 121).

$\Phi_{Fi} = E_{fi} - E_f = -kT/e\ln(Nd/ni)$ (V-12) where Efi and ni are respectively the Fermi level and the intrinsic concentration.

For $0>Vs>2\Phi_{Fi}$, Qsc is negative and it is the depletion mode and low inversion:

$$Qsc \approx \frac{\varepsilon skT}{eLd}\sqrt{\frac{eVs}{kT}} \quad \textbf{(V-13)}$$

V.3.5.3. Different conductor areas of nanowire:

When we apply a bias at the drain, the surface potential is modified along the nanowire. Thus, we can encounter the different regimes (accumulation and depletion) on different areas of the nanowire. The surface potential Vs(x) at the distance x from the source is given by Vs(x)=(Vsbg-Vsfb)+V(x) (V-14). Vsbg and Vsfb are respectively the surface potential related to Vbg and Vfb. The potential Vds is along the wire. At x, this potential is equal to V(x).

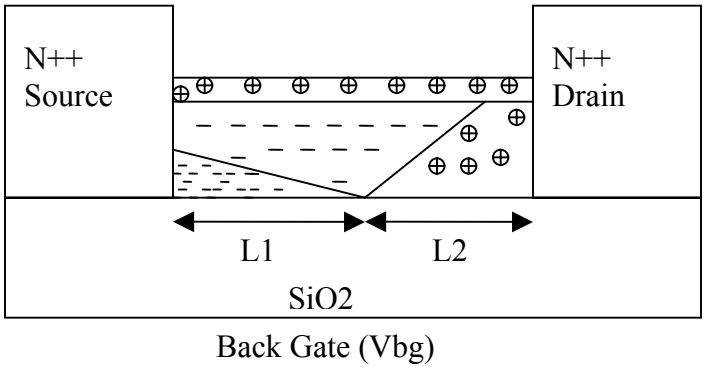


Figure V-34: cross section with the different areas of the wire.

We can model the nanowire as a combination of several resistance (figure V.34): R1 for accumulation with a length L1, R2 for depletion with a length L2.

V.3.5.4. Calculation of V(L1), transition between accumulation and depletion:

We have to determine the length of L1 and L2 of accumulation and depletion region. At the transition between both regions, the accumulation charge $Qacc(L1) = 0$ and so V(L1)=Vbg-Vfb. The accumulation charge at a distance x from the source is Qacc=Cox*(Vbg-Vfb-V(x)) (V-15).

V.3.5.5. Accumulation region:

As the substrate is p type and the nanowire type n, both are in accumulation for V(x)<V(L1) (figure V-35)

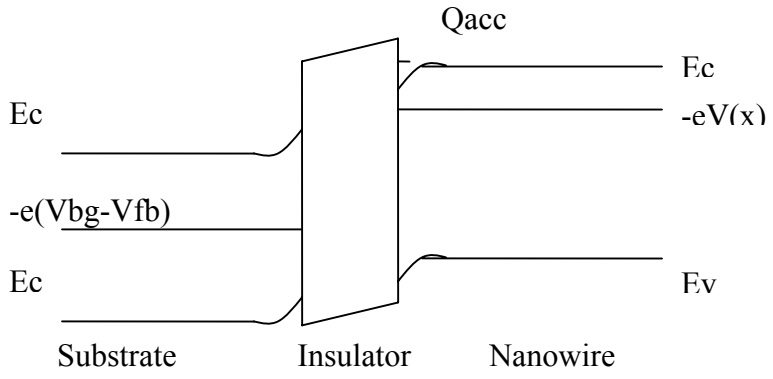


Figure V-35: Energy band diagram for V(x)<V(L1)

Qacc=Cox*(Vbg-Vfb-V(x)) (V-16)

V(x)<Vbg-Vfb. It is just a capacity, so to get the current only Qacc is required:

$$Id.dx = -2r.\mu.Qacc(x).dV = 2r.\mu.Cox.((Vbg - Vfb) - V(x))dV \text{ .(V-17)}$$

Thus, $Id_{acc} = 2r\mu Cox / 2L * (2(Vbg - Vfb) - Vds)Vds$ in case where Vds<V(L1), that is to say when the region L2 doesn't exist.

Otherwise, $Id_{acc} = 2r\mu Cox / 2L * (Vbg - Vfb)^2$ in saturation case Vds>V(L1).

The variation of accumulation current for low Vds are given in the following graph (figure V.35). The current is stronger for low doping which is due to the mobility dependence. Nss* has been chosen at $5.10^{11} cm^{-2}$ and Vbg=30V, L=1um and r=10nm.

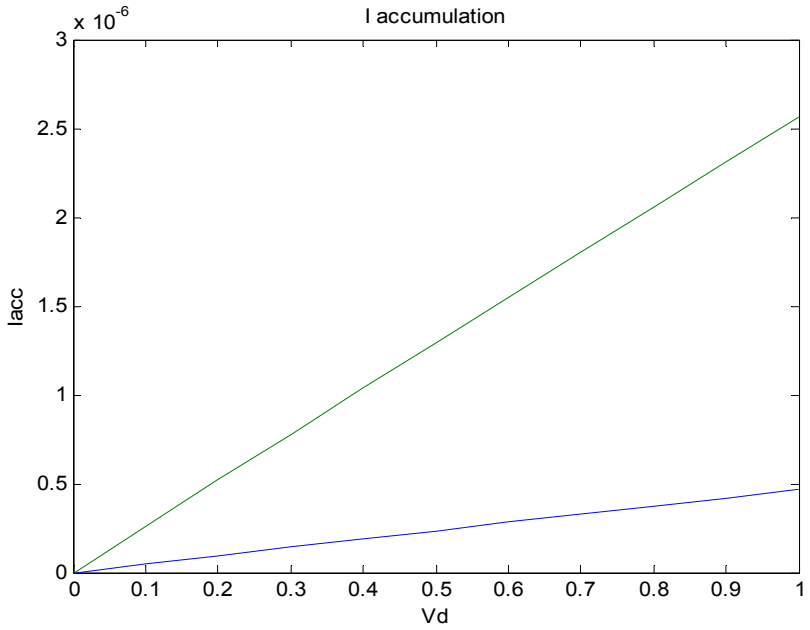


Figure V-36: Ids(A)-Vds(V) in accumulation for Vbg=30V, $Nss^* = 5.10^{11} cm^{-2}$, L=1um and r=10nm. The two curves are for two dopings: $Nd = 2.10^{17} cm^{-3}$ (upper curve) and $Nd = 10^{19} cm^{-3}$.

The figure below highlights the mobility saturation effect which is not negligible in our case (Figure V-37).

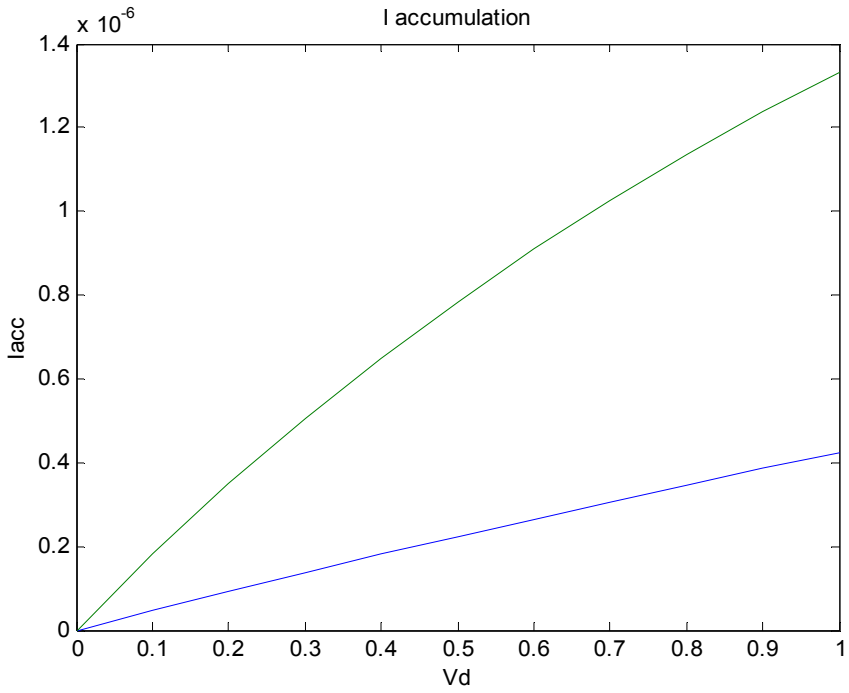


Figure V-37: Ids(A)-Vds(V) in accumulation with saturation with the same characteristics as the previous curve.

If we take $Nss \sim 10^{12}\,cm^{-2}$ and Nss*=f(Nd, Nss) figure V-38, the current decrease for $Nd = 10^{19}\,cm^{-3}$ compared to previous simulation. This is due to the flat band bias Vfb depends on Nss*.

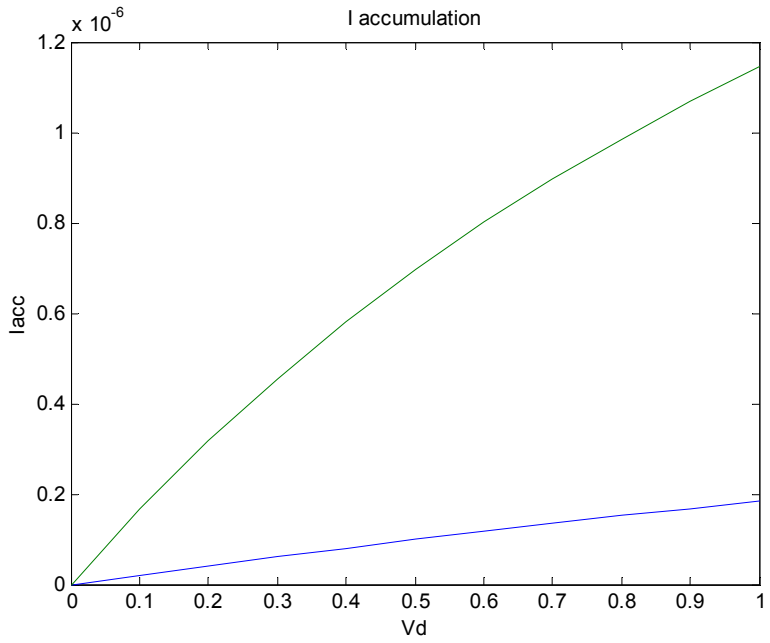


Figure V-38: Iacc(A), accumulation current with Vds for different doping, $Nss = 10^{12}\,cm^{-2}$ and Nss*=f(Nss,Nd)

For a doping fixed at $2.10^{17}\,cm^{-3}$ and the same parameter as previously, the figure V-39 highlights the modulation effect of accumulation current for gate bias Vbg=15, 25, 35 and 45V from the bottom

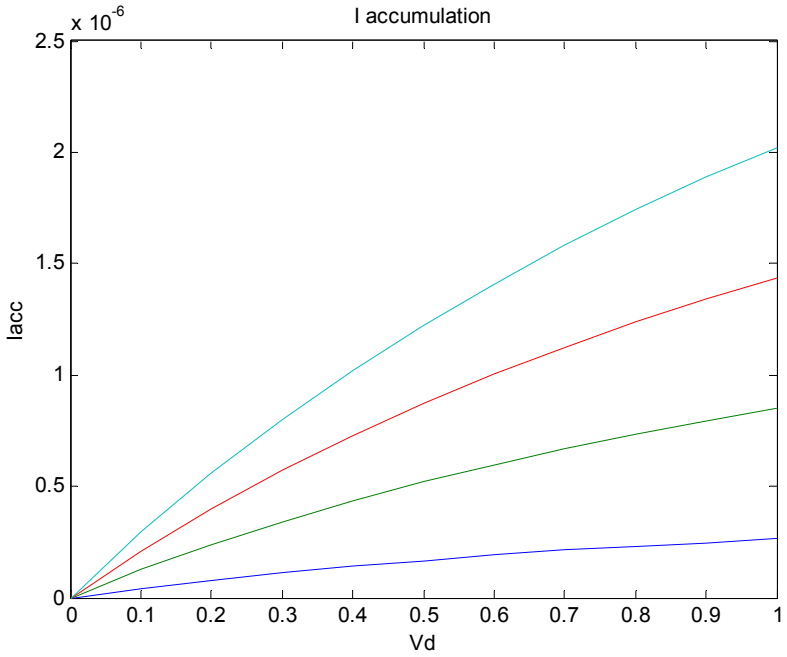


Figure V-39: Iacc(A) accumulation current with Vds for Nd=$2.10^{17}\,cm^{-3}$ and Vbg=15, 25, 35 and 45V (from the bottom).

Without taking into account the mobility saturation, the curves are linear for low Vds. For higher Vds, we can reach the pinch off and so the saturation regime. The following curve (figure V-40) shows the saturation effect related to pinch off for $Nd = 2.10^{7}\,cm^{-3}$ and for Vbg=15, 25V.

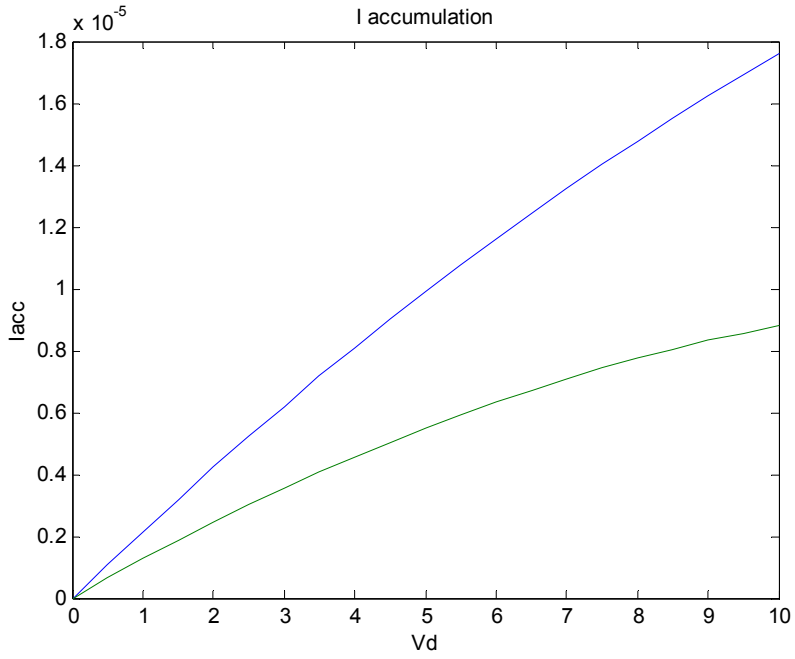


Figure V-40: Saturation effect related to channel pinch for $Nd = 2.10^{7}\,cm^{-3}$ and Vbg=15, 25V (from bottom).

If we consider the saturation of mobility, the non-linearity appeared before 1V (figure V-41).

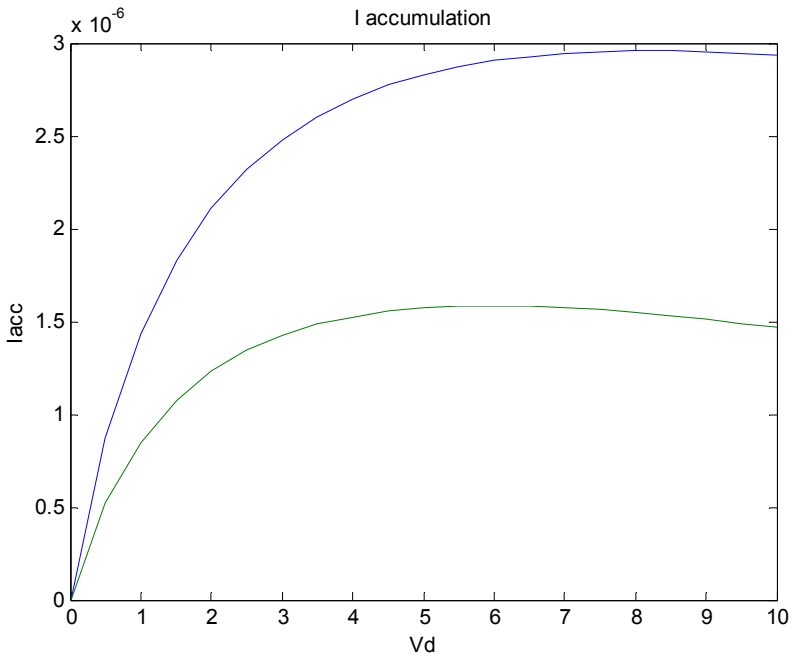


Figure V-41: Both saturation effect of mobility and channel pinch for $Nd = 2.10^7\, cm^{-3}$ and Vbg=15, 25V.

If we chose $Nd = 10^{19}\, cm^{-3}$ and Vbg=15, 25 and 35V, the mobility saturation comes later because it is lower (figure V-42).

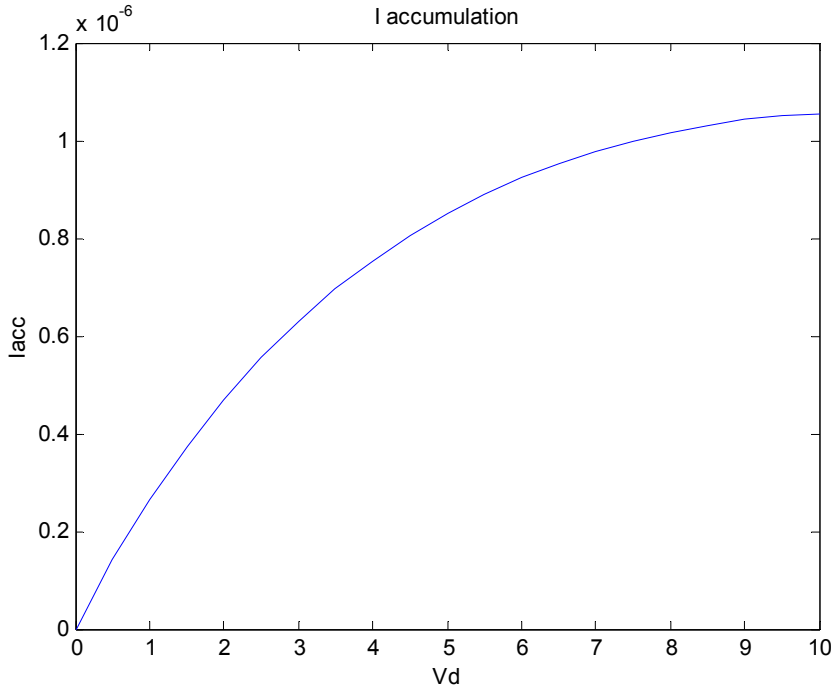


Figure V-42: Both saturation effect of mobility and channel pinch for Vbg=30V and Nd=$10^{19}\,cm^{-3}$.

The accumulation charge begins for Vbg=Vfb then increase exponentially. The curve I-Vbg for Vds=0.1V, 1V and 5V (from the bottom) shows this effect (figure V-44) and allows to determine precisely Vfb experimentally based on the log curve (figure V-43).

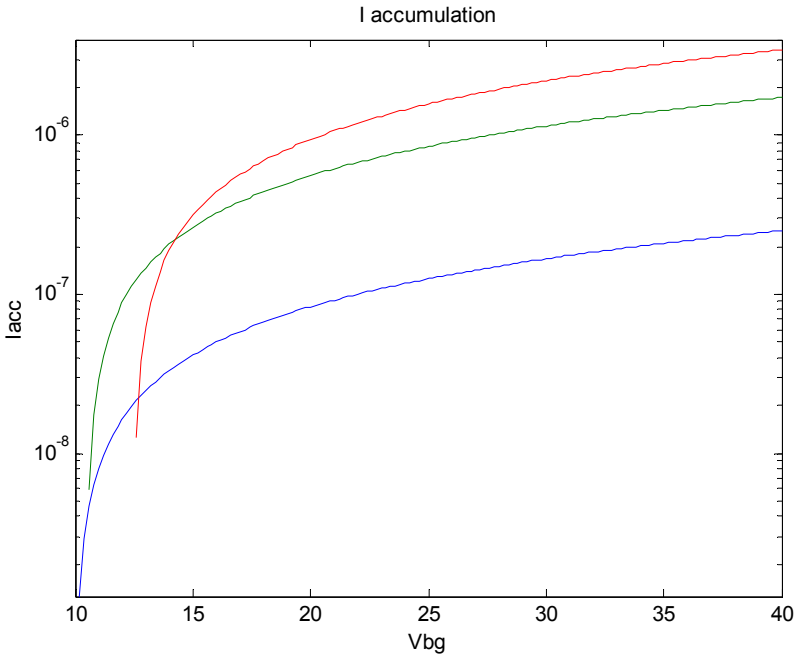


Figure V-43: Iacc(A)-Vbg(V) in log scale for $Nd = 2.10^{7}\,cm^{-3}$ and Vbf~10V.

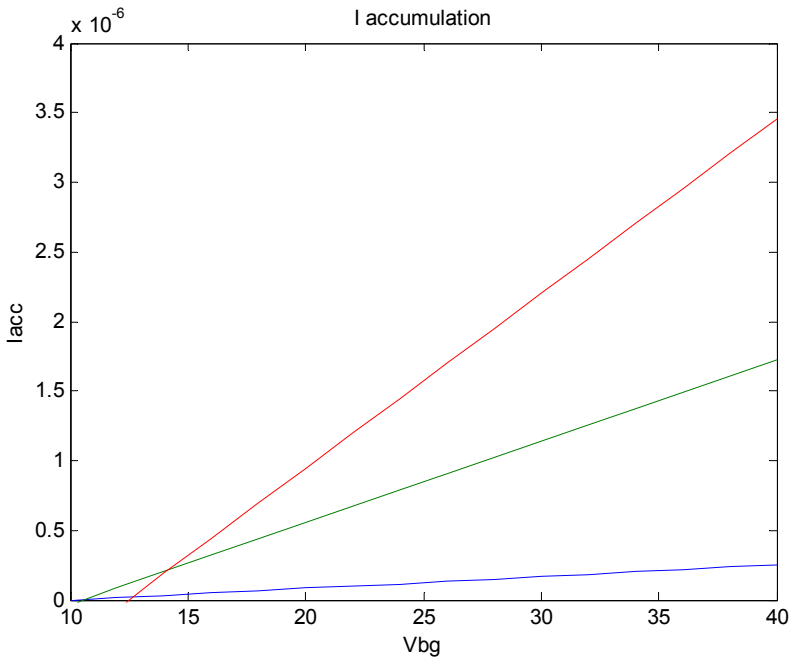


Figure V-44: Iacc(A)-Vbg(V) for $Nd = 2.10^7 cm^{-3}$ and Vds= 0.1, 1, 5V.

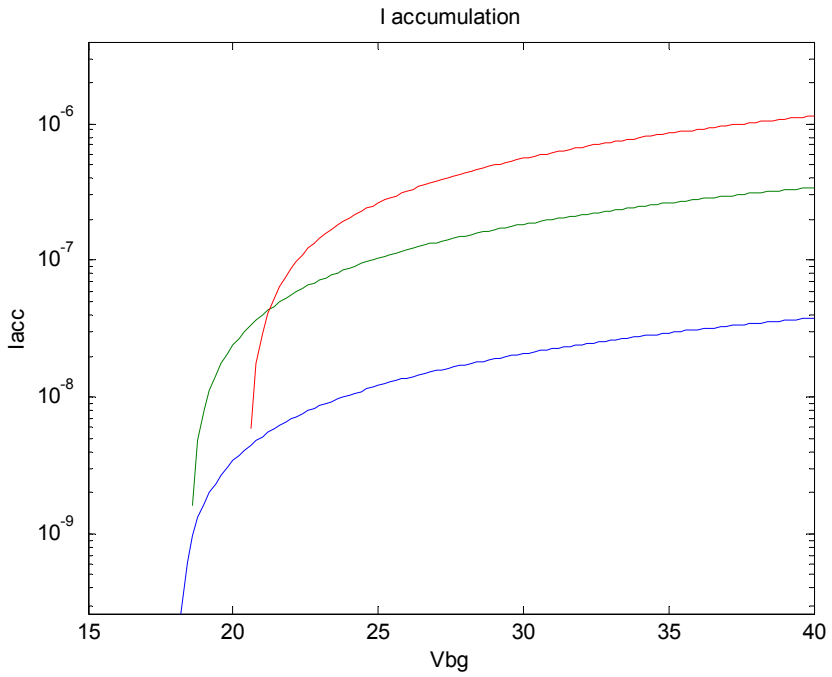


Figure V-45: Iacc(A)-Vbg(V) in log scale for $Nd = 2.10^7 cm^{-3}$ and Vbf~22V.

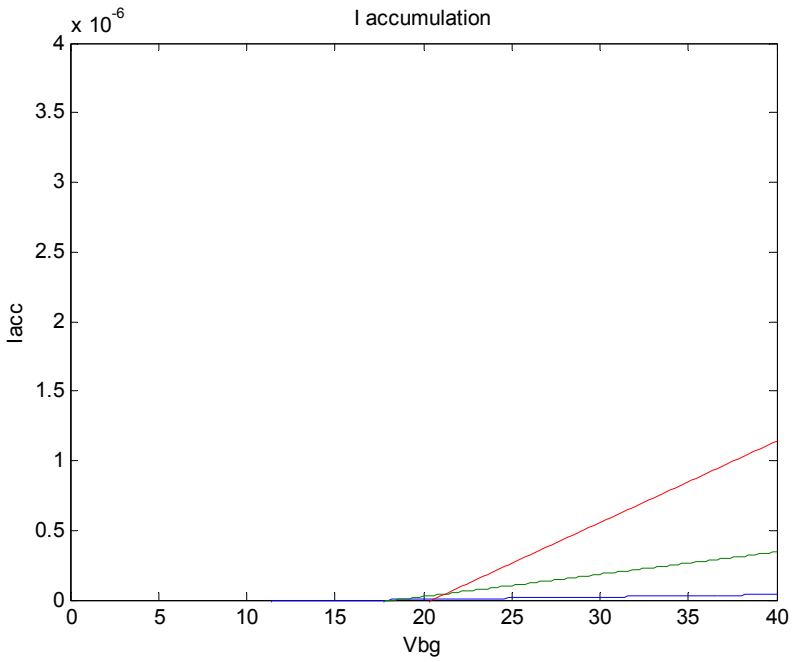


Figure V-46: Iacc-Vbg for $Nd = 10^{19}\,cm^{-3}$ and Vds=0.1, 1, 5V.

Thus, it is necessary to compare the spread of the accumulation with the nanowire dimension. The Debye length is the characteristic length of the accumulation charges. It is related to the dielectric relaxation time with: $Ld = \sqrt{D\tau_r} = \sqrt{\frac{\varepsilon kT}{e^2 Nd}}$ (V-18)

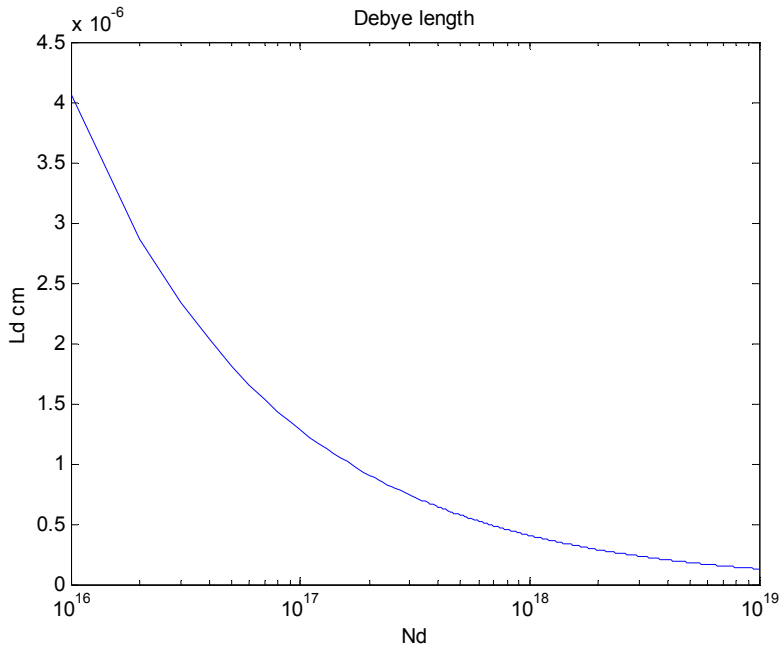


Figure V-47: Debye Length with Nd

The Debye length is a function of the doping concentration Nd. The above figure shows that this length is higher than the radius of our nanowires for Nd<$10^{17}\,cm^{-3}$, it is about 7nm for $2.10^{17}\,cm^{-3}$ and is about1nm for $10^{19}\,cm^{-3}$.

V.3.5.6. Parallel resistance:

With the accumulation region, some current flows inside the nanowire, according to the depleted region caused by the interface states. In this case, the nanowire behaves like a JFET with a modulation of the conductor section through (Vds, Vbg, Vfb) in series with R1wire. If the nanowire is in accumulation (L1>L) so the wire can be seen as two resistances in parallel Racc/R1wire.

Given $Seff = \pi r_{eff}^2$ the effective section and σ the conductivity, the conductance related to R1 is $G1wire = \sigma * S / L = Nd.e.\mu_n.\pi r_{eff}^2 / L1$ (V-19)

We have established the relation between Ldep, Nd and Ns in the previous paragraph. For Nss>$10^{11} cm^{-2}$ and Nd= $2.10^{17} cm^{-3}$ Ldep>10nm so G1wire=0. This result gives much information on the transport in nanowire for this doping. Indeed, the nanowire is naturally depleted because of the interface states. For Vbg>Vfb, an accumulation layer appears at the lower interface turning into On the circuit. It is similar to a MOS transistor. On the one hand, the circuit turns from isolator into a conductor after the formation of inversion layer for Vg>Vt called threshold voltage. Consequently, the simulation of Iacc for $Nd = 2.10^{7} cm^{-3}$ in the previous part corresponds to Ids in a nanowire. The drawback is the thickness of the insulator between the wire and the bias is high, thus Capacity is low. This induces a dependence of this term on the interfaces charges which is predominant for Vfb and thus Vfb can vary a lot from one device to another.

For higher doping, especially Nd=$10^{19} cm^{-3}$, Ldep<10nm and so G1 is not equal to zero. The following figure shows the calculation I=G1.Vds for Ldep=0, 3, 6 and 9nm. We have taken into account the mobility saturation which is low for this doping. We should notice that Vfb<Vbg<Vfb+40V, IR1/Iacc>10: transport is essentially due to the nanowire conductivity (figure V-48).

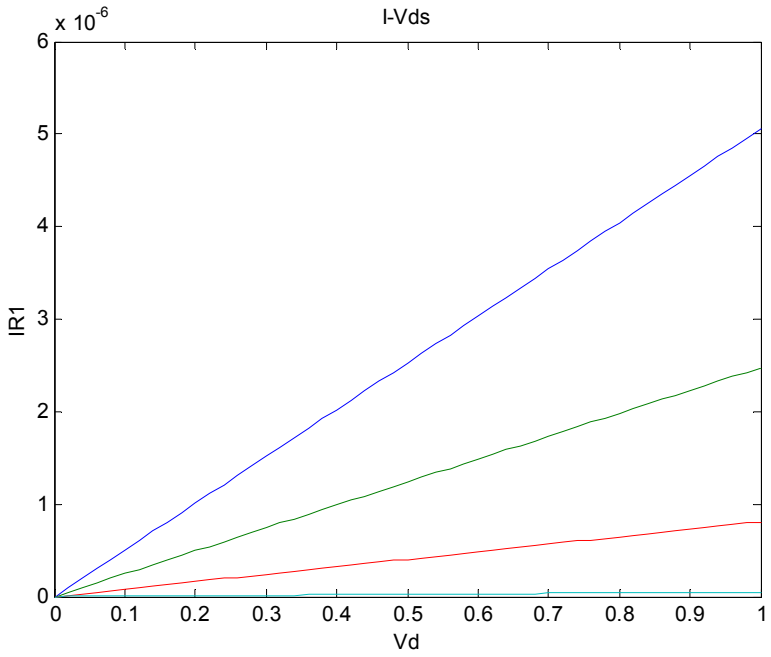


Figure V-48: I-Vds of parallel current to accumulation layer in case of $Nd = 10^{19} cm^{-3}$ for d=0, 3, 6, 9nm from the bottom.

For this simulation, we have considered that the mobility of electrons in the nanowires is the same as in the bulk. However, it is decreased by the FS effect.

V.3.5.7. Depletion area:

We have seen that V(L1)=Vbg-Vfb determines the transition between the accumulation and depletion region in the wire. Thus, in the case where V(L1)<Vds, there is a depletion region in the wire which is all more important since V(L1) is weak.

The difference of doping between substrate and the wire makes the wire enter in depletion with back-gate substrate. Thus, the bias applied on the gate is divided between two space charge regions (Wdep1 and Wdep2). It is possible to establish a link between both with electro-negativity between Qdep of charge space region from back gate and

from wire. Indeed, $Qdep(\Psi s1, Na) = Qbg = -Qn = Qdep(\Psi s2, Nd)$ with $\Psi s1$ and $\Psi s2$ the surface potential of back gate and wire respectively, Na p type doping of back-gate and Nd n-type of wire.

$$Qdep = \rho Wdep = eNd\sqrt{\frac{-2\varepsilon\Psi s2}{eNd}} = eNa\sqrt{\frac{2\varepsilon\Psi s1}{eNa}} \quad \textbf{(V-20)}$$

So, $\Psi s2 = -Na/Nd * \Psi s1$. But $\Psi s1inversion = 2kT/e\ln(Na/ni)$=0.476V. Thus there is a strong inversion at the back side as soon as $\Psi s2 = 3.10^{-5} V$. This low value comes from that the back gate substrate is nearly intrinsic.

Thus, $[Vbg - Vfb + \Psi s1inv - V(x)] = Vox + \Psi s2$ (V-21). By setting $\Psi s1inv$ to Vfb*=Vfb-$\Psi s1inv$, we get $[Vbg - Vfb* - V(x)] = Vox + \Psi s2$ (V-22) which is the MOS capacity equation.

We set Vbg-Vfg*-V(x)=Veq **(V-23)**

$$Veq = -\frac{1}{Cox}\sqrt{2\varepsilon eNd}\sqrt{-\Psi s2} + \Psi s2 \quad \textbf{(V-24)}$$

By setting $X = \sqrt{-\Psi s2}$, we got the following equation:

$X^2 + bX + c$ with $b = -\frac{1}{Cox}\sqrt{2\varepsilon eNd}$ and c=-Veq

The discriminant $\Delta = b^2(1 + 4Veq/b^2)$

As b~-220 for $Nd = 10^{19} cm^{-3}$, we can consider that $Veq/b^2 << 1$, Thus

$(\Delta)^{1/2} = b(1 + 2Veq/b^2)$ and $\sqrt{-\Psi s2} = X = -b/2 + b/2 + Veq/b = -\frac{Cox}{\sqrt{2e\varepsilon Nd}}Veq$

Consequently, $Wdep(x) = \sqrt{\frac{2\varepsilon(-\Psi s2)}{eNd}} = -Cox.Veq / eNd$ (V-25). This result highlights the previous approximation which is to neglect the spread of the charge space region in case the capacity is low.

Finally Wdep(x)=Cox.(V(x)+Vfb*-Vbg)/eNd (V-26)

The determination of the current is now similar to this of a JFET by integrating the non depleted region along the wire.

The current depends directly on the thickness of the depleted region. The calculation is in function of the surface potential (figure V.49) and shows that the saturation phenomenon of the spread of the charge space region. This can be related to the apparition of the strong inversion when the surface potential of the wire reaches the inversion $\Psi s2inv = 2kT / e \ln(Nd / ni)$

We can note that the maximal spread of the deleted region is $Wdep\max = \sqrt{\frac{2\varepsilon\Psi s2inv}{eNd}}$

for $Nd = 10^{19} cm^{-3}$ doesn't allow to pinch totally the wire to reach the saturation of current as in the JFET. The evolution of Wdepmax=f(Nd) is shown as below (figure V.50). The spread decreases with the doping. Finally, figure V.51 shows Wdep=f(Vbg) for Vds=0. The low capacity of Cox doesn't allow the wire to reach the saturation.

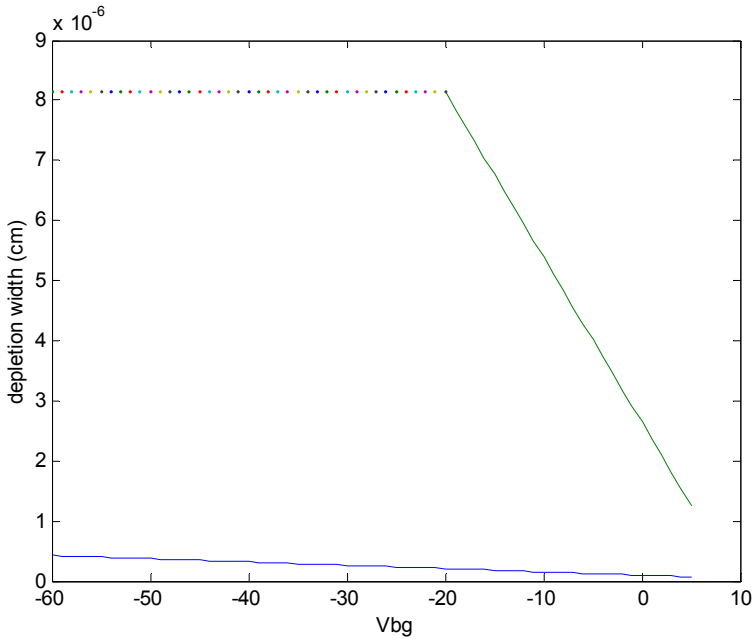


Figure V-49: evolution of the depletion width with Vbg (V) for $Nd = 10^{19}\,cm^{-3}$ (lower curve) and for $Nd = 2.10^{7}\,cm^{-3}$. Vds=0

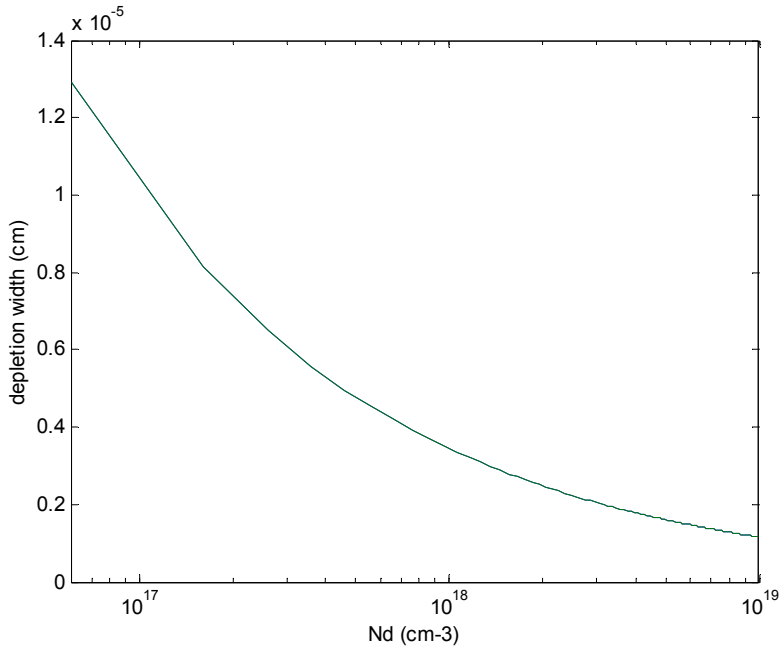


Figure V-50: Maximum depletion width with the doping Nd(cm^{-3}).

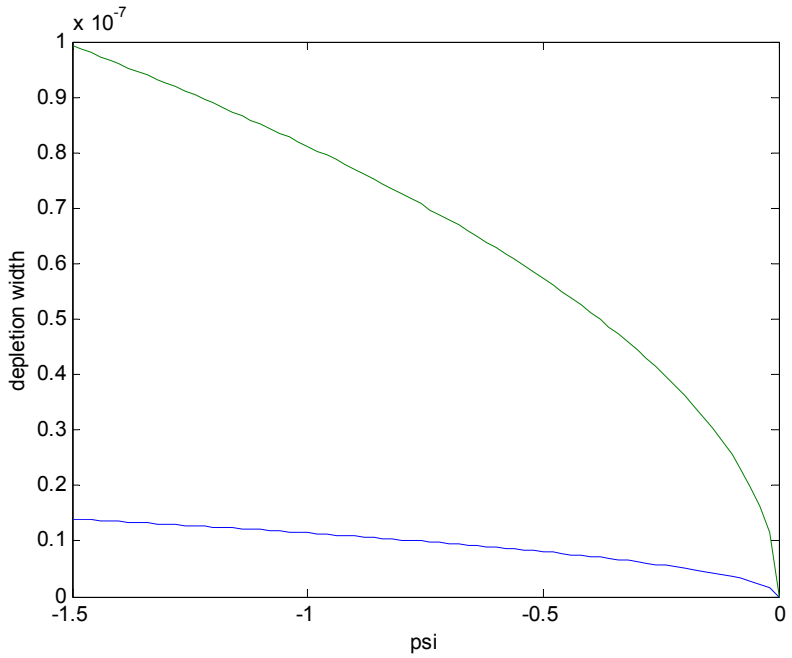


Figure V-51: Evolution of the depletion width (cm) with the surface potential for $Nd = 10^{19}\,cm^{-3}$ (lower curve) and for $Nd = 2.10^{7}\,cm^{-3}$.

We can now determine Ids. In case where Wdep=0, the conductance in the depletion region can be written as follow:

$$G_{02} = \sigma.(\pi(r-d)^2)/(L-L1)$$

$$I(x) = \sigma.(\pi(r-d-Wdep(x)^2)/(L-L1)dV/dx$$

$$I(x)dx = G_{02}(L-L1)(1-2*\frac{Wdep(x)}{1-d}+(\frac{Wdep(x)}{1-d})^2)dV \quad \textbf{(V-27, V-28, V-29, V-30, V-31)}$$

$$I(x)dx = Go/L1*(1-\frac{(V(x)+Vfb-Vbg)}{\Psi})dV$$

$$1/\Psi = Cox/(e.Nd.(r-d))$$

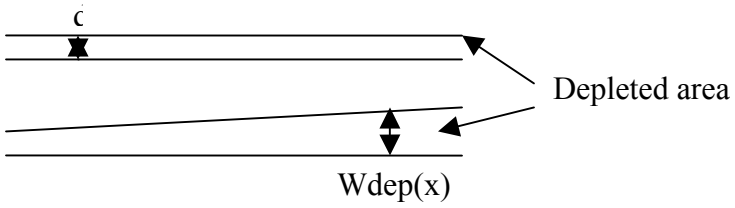


Figure V-52: Cross section of a nanowire with depleted area.

We have neglected the second order effects in the previous equation.

We should integer between 0 and Vds:

$$Ids = GoVds - GoVds * [(Vds + 2(Vfb - Vbg)] / 2\Psi \quad \textbf{(V-32)}$$

Simulations of I-V and I-Vbg related to this equation for $Nd = 10^{19} cm^{-3}$ are drawn above figure V.53 and V.54. First one shows Ids-Vds taking into account the accumulation current equal to zero. Gate effect is low since the spread of the depleted region is weak with bias at this doping. The mobility saturation is taken into account and can not be neglected for V>1V. There is no saturation effect like JFET because we can not reach the pinch off at this doping.

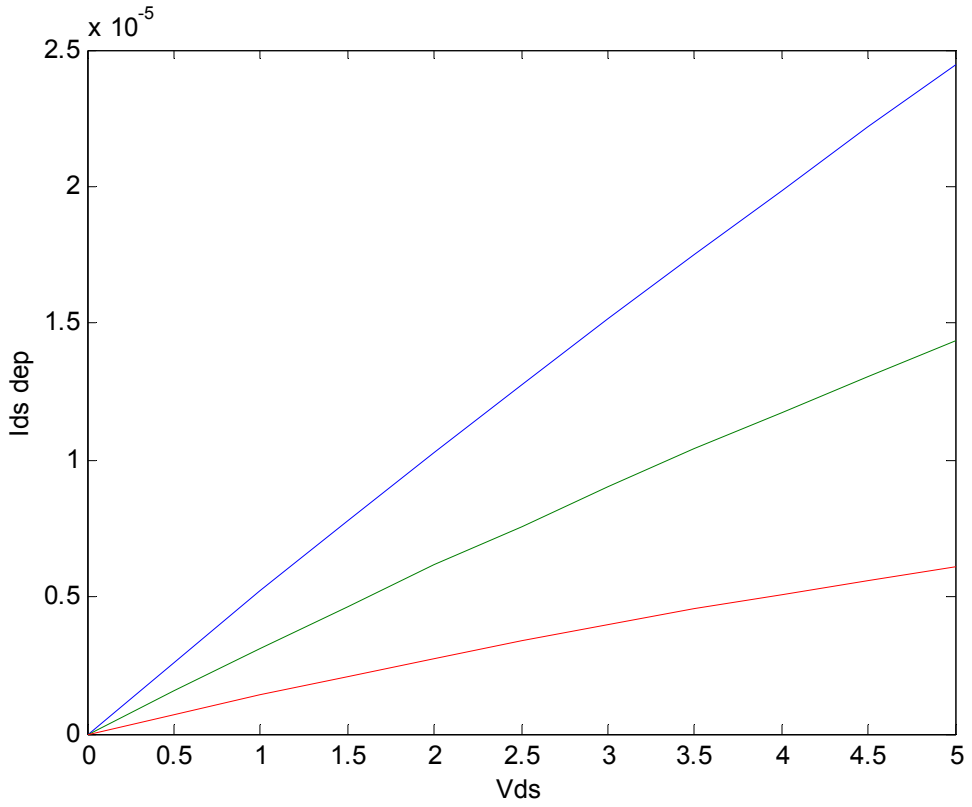


Figure V-53: Ids(A)-Vds(V) in depletion area for Vbg=20V, 0,-20V and $Nd = 10^{19} cm^{-3}$

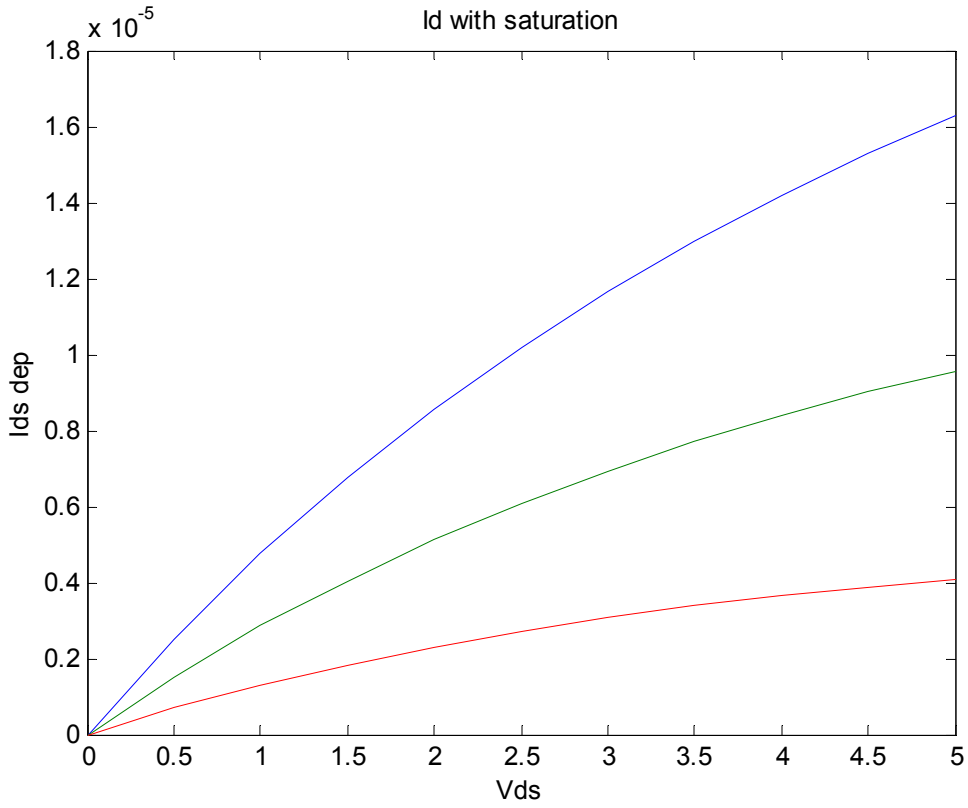


Figure V-54: same simulation with the mobility saturation.

V.4. Conclusion:

So, the transport in nanowires is complex. Indeed, the space charge region induced by the interface states turns the wire into an insulator at room temperature. Thus, we need to apply a back-gate higher than the flat band potential to reach the accumulation region and to turn the wire conductor. Only the section at the interface with the buried oxide induces a current through the accumulation layer.

For higher doping $Nd = 10^{19} cm^{-3}$, the wire is naturally conductor even for gate bias lower than the flat band potential. It is impossible to turn the wire into insulator even by applying a strong negative bias because the maximal spread around the radius of the

nanowire. It behaves like a JFET with modulation of the conductor section along the wire. When the back gate bias is higher than the potential of flat band, so the accumulation layer induces a current in parallel. But the accumulation current values are lower with one order magnitude for this doping, the conduction in the wire is predominant. Eventually, we have to remember that these simulations have been done under classical physics and don't take into account the effect of quantum mechanics.

Conclusion:

During my journey in SNDL Lab at the National University of Singapore for the double degree program with French University, even if we didn't get the fund to start the experiment during my length of stay here, we have set up the basis to begin this new project.

First, we have reviewed the motivations which have lead us to think about this new device. Thus, Nanowires-FET appeared to be an interesting device to enter in the quantum area and which would enable us to overcome hurdles that others devices have to deal with.

Then, we have set up the recipe to grow nanowires and build nanowires. We have reviewed different methods and chosen one: VLS method. Then as for the process, two ways are possible, either to use a microscope to localize a suitable nanowire and define subsequently the device; or to align nanowires on a large area and to follow the normal flow.

Finally, we have applied the classical physics to understand the mechanism of transport through a nanowire according to the doping concentration and the density of interface state. Still, this simulation doesn't take into account the quantum mechanisms that are important at this scale.

This new device may unveil surprising electrical results. Even if we have explained their way of working with an analogy with JFET, the nanowires-FET due to this dimension may involve other phenomena due to the one dimension quantum confinement. For example, if we can apply a constriction on the nanowire, this device due to this dimension can experience the Coulomb Blockade phenomenon which may allow to reach

the development of the Single Electron Transistor working at higher temperature than the other device built up to now. (Appendices B for explanation)

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Appendices:

A.1: non linear equation resolution:

Referring to the equation V.8, the resolution requires a computation to get the result. To handle this, we used Matlab 6 to get the zeroes of this equation through the two following program:

```
function x=fff(N)
Nestim = 3
x=fzero(@ftmpbis,Nestim,[],N);
```

```
function y = ftmpbis (x, N)
y = 1./(1.+7.46e-4*exp(x.^2))-2.54e11*N.^-1*x;
```

All the other equations used the results coming from these two equations. Then we draw the graph through the software Origin. So, figures V.23 to V.31 used the previous results.

A.2: Curve from linear equation:

As for the others, we can quote some programs written in Matlab as well. I will quote some, all the other use the same scheme, we just modified the variable:

- **Depletion V.25:**

```
u=-1.5:0.02:0
y1=sqrt(2*11.9*8.85e-12*-u./(1.6e-19*1e25))
y2=sqrt(2*11.9*8.85e-12*-u./(1.6e-19*2e23))
plot(u,y1,u,y2)
xlabel('psi')
ylabel('depletion width')
```

- **Depletion V.49:**

```
u=6e16:100000000000000000:1e19
y1=sqrt(2*11.9*8.85e-14*2*0.025*log(u./1.5e10)./(1.6e-19*u))
y2=sqrt(2*11.9*8.85e-14*2*0.025*log(u./1.5e10)./(1.6e-19*u))
semilogx(u,y1,u,y2)
xlabel('Nd (cm-3)')
ylabel('depletion width (cm)')
```

```
xlim([6e16 1e19])
```

- **Depletion V.51:**

```
u=-20:1:5
y1=8.8e-9*(17.6-u)./(1.6e-19*1e19)
y2=8.8e-9*(9.6-u)./(1.6e-19*2e17)
plot(u,y1,u,y2)
xlabel('Vbg')
ylabel('depletion width (cm)')
hold('on')
u=-60:1:-20
y3=8.8e-9*(17.6-u)./(1.6e-19*1e19)
y4=8.14e-6
plot(u,y3,u,y4)
```

- **Ids-Vbg with saturation V.54:**

```
u=-40:25
y1=0.1.*1e19.*1.6e-19.*100.*3.16.*(10e-7-[8.85e-9.*(0.1+17.6-u)./(1.6e-
19.*1e19)]).^2/(1e-4)-0.1.*1e19.*1.6e-19.*100.*3.16.*(10e-7-[8.85e-9.*(0.1+17.6-
u)./(1.6e-19.*1e19)]).^2/(1e-4).*[0.1+2.*(18-u)].*8.85e-9./(1.6e-19.*1e19.*(10e-7-
[8.85e-9.*(0.1+17.6-u)./(1.6e-19.*1e19)]))
y2=1.*1e19.*1.6e-19.*100.*3.16.*(10e-7-[8.85e-9.*(1+17.6-u)./(1.6e-
19.*1e19)]).^2/(1e-4)-1.*1e19.*1.6e-19.*100.*3.16.*(10e-7-[8.85e-9.*(1+17.6-u)./(1.6e-
19.*1e19)]).^2/(1e-4).*[1+2.*(18-u)].*8.85e-9./(1.6e-19.*1e19.*(10e-7-[8.85e-
9.*(1+17.6-u)./(1.6e-19.*1e19)]))
y3=5.*1e19.*1.6e-19.*100.*3.16.*(10e-7-[8.85e-9.*(5+17.6-u)./(1.6e-
19.*1e19)]).^2/(1e-4)-5.*1e19.*1.6e-19.*100.*3.16.*(10e-7-[8.85e-9.*(5+17.6-u)./(1.6e-
19.*1e19)]).^2/(1e-4).*[5+2.*(18-u)].*8.85e-9./(1.6e-19.*1e19.*(10e-7-[8.85e-
9.*(5+17.6-u)./(1.6e-19.*1e19)]))
plot(u,y1,u,y2,u,y3)
xlabel('Vbg')
ylabel('Ids dep')
Title('Id ')
```

B: Coulomb Blockade phenomenon:

To understand the conclusion concerning the Coulomb Blockade, let us calculate the dimension required to experience this phenomenon at room temperature.

The charge/tension characteristic of coulomb Blockade phenomenon is possible at the following condition: the electrostatic energy quantum $e^2/2C$ must be superior to the thermal energy k_BT. In case where $e^2/2C << k_BT$, it is not anymore the bias applied to

source/drain of the device which control the energy supply to allow electron to flow. It is the thermal energy which is a random process. Thus, we lose the control on the charge supply to the condensator.

To be able to see the quantification phenomenon, it is required that:

$$\frac{e^2}{2C} >> k_B T$$

A numerical application at room temperature gives us the following constraint on the value of the capacity:

$$\frac{e^2}{2C} >> k_B T \Rightarrow C << \frac{e^2}{2k_B T}$$

That means the atto-Farad as magnitude of order (1 aF=$10^{-18} F$)

C<<1aF

Now if we try to determine the dimension associated to this capacity, that we would modelize by a plan condensator (with surface S, isolator thickness e_{ox} and relative permittivity ε) so that:

$$C = \frac{\varepsilon \varepsilon_0 S}{e_{ox}} \sim \varepsilon_0 d$$

We get as characteristic dimension d of the systems:

$d < 10nm$

This is the diameter of the nanowires we would like to grow.